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IEEE Standard for Ethernet

Amendment 5: Physical Layers Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3cg™-2019
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018,
IEEE Std 802.3bt™-2018, IEEE Std 802.3cd™-2018,
and IEEE Std 802.3cn™-2019)

IEEE

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Approved 7 November 2019

IEEE SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2018 specifies additions and appropriate modifications to add 10 Mb/s Physical Layer (PHY) specifications and management parameters for operation, and associated optional provision of power, over a single balanced pair of conductors.

Keywords: 10BASE-T1L, 10BASE-T1S, amendment, copper, Ethernet, IEEE 802.3™, IEEE 802.3cg™, MASTER-SLAVE, medium dependent interface, physical coding sublayer, Physical Layer, Physical Layer Collision Avoidance, PLCA, physical medium attachment

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Introduction

This introduction is not part of IEEE Std 802.3cg-2019, IEEE Standard for Ethernet—Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of publication for IEEE Std 802.3cg-2019, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb™-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt™-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

IEEE Std 802.3cn™-2019

Amendment 4—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds 50 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications and management parameters for operation over single-mode fiber with reaches of at least 40 km.

Amendment 5—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 146 through Clause 148 and Annex 146A and Annex 146B. This amendment adds 10 Mb/s Physical Layer specifications and management parameters for operation on a single balanced pair of conductors.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018, IEEE Std 802.3bt™-2018, IEEE Std 802.3cd™-2018, and IEEE Std 802.3cn™-2019.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.[1]

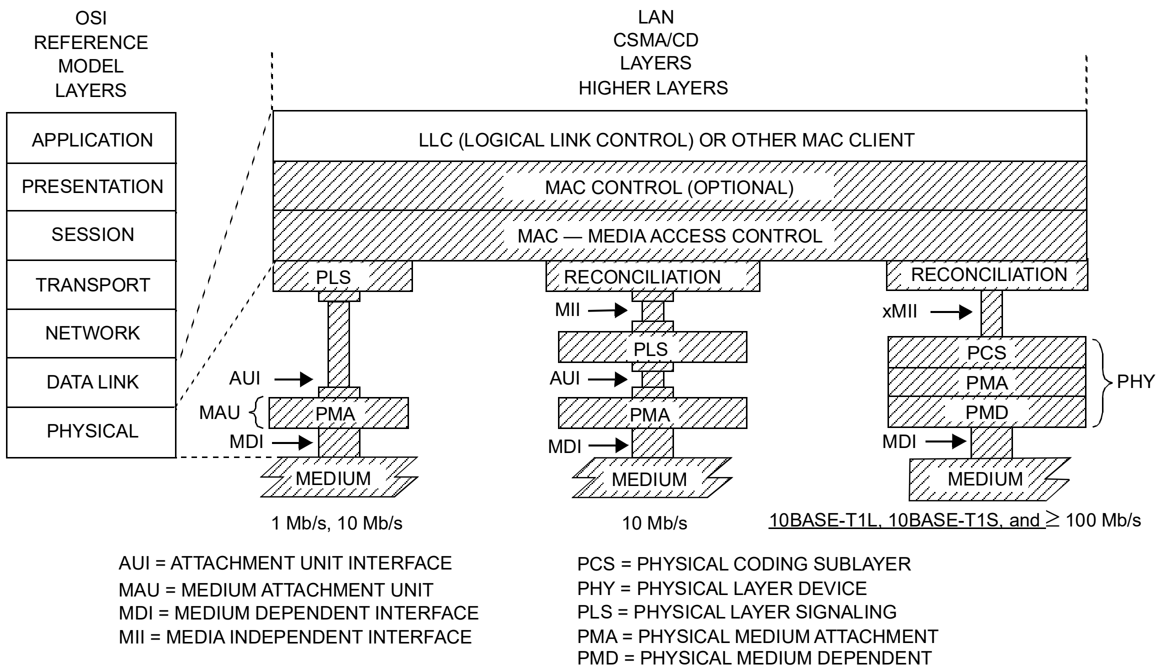
[1] Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

Change Figure 1–1 as follows (see changes at the bottom of the right column and in the note):



NOTE—In this figure, the xMII is used as a generic term for the Media Independent Interfaces for implementations of 10BASE-T1L, 10BASE-T1S, and 100 Mb/s and above. For example: for 100 Mb/s implementations this interface is called MII; for 1 Gb/s implementations it is called GMII; for 10 Gb/s implementations it is called XGMII; etc.

Figure 1–1—IEEE 802.3 standard relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

1.3 Normative references

Insert the following references in alphanumeric order:

IEC 60068-2-2:2007, Environmental testing—Part 2-2: Tests—Test B: Dry heat.[2]

IEC 60068-2-6:2007, Environmental testing—Part 2-6: Tests—Test Fc: Vibration (sinusoidal).

IEC 60068-2-14:2009, Environmental testing—Part 2-14: Tests—Test N: Change of temperature.

IEC 60068-2-31:2008, Environmental testing—Part 2-31: Tests—Test Ec: Rough handling shocks, primarily for equipment-type specimens.

[2]IEC publications are available from the International Electrotechnical Commission (http://www.iec.ch/). IEC publications are also available in the United States from the American National Standards Institute (http://www.ansi.org).

IEC 60079-0:2017, Explosive atmospheres—Part 0: Equipment—General requirements.

IEC 60079-11:2011, Explosive Atmospheres—Part 11: Equipment protection by intrinsic safety.

IEC 60529:2013, Degrees of Protection Provided by Enclosures (IP Code).

IEC 61000-4-4:2012, Electromagnetic compatibility (EMC)—Part 4-4: Testing and measurement techniques—Electrical fast transient/burst immunity test.

IEC 61000-4-5:2017, Electromagnetic compatibility (EMC)—Part 4-5: Testing and measurement techniques—Surge immunity test.

IEC 61000-4-6:2013, Electromagnetic compatibility (EMC)—Part 4-6: Testing and measurement techniques—Immunity to conducted disturbances, induced by radio-frequency fields.

IEC 61000-6-4:2018, Electromagnetic compatibility (EMC)—Part 6-4: Generic standards—Emission standard for industrial environments.

IEC 61010-1:2017, Safety requirements for electrical equipment for measurement, control, and laboratory use—Part 1: General requirements.

IEC 61326-1:2012, Electrical equipment for measurement, control and laboratory use—EMC requirements—Part 1: General requirements.

IEC 62368-1:2014, Audio/video, information and communication technology equipment—Part 1: Safety requirements.

ISO 4892:1982, Plastics—Methods of exposure to laboratory light.[3]

NAMUR NE 021:2017, Electromagnetic Compatibility of Equipment for Industrial Processes and Laboratory.[4]

1.4 Definitions

Insert the following new definitions after 1.4.50 "10BASE-T":

1.4.50a 10BASE-T1L: IEEE 802.3 Physical Layer specification for a 10 Mb/s Ethernet local area network over a single balanced pair of conductors up to at least 1000 m reach. (See IEEE Std 802.3, Clause 146.)

1.4.50b 10BASE-T1S: IEEE 802.3 Physical Layer specification for a 10 Mb/s Ethernet local area network over a single balanced pair of conductors up to at least 15 m reach. (See IEEE Std 802.3, Clause 147.)

Change 1.4.151 as follows:

1.4.151 BASE-T1: PHYs that belong to the set of specific Ethernet PCS/PMA/PMDs that operate on a single twisted-pair copper cable, including 10BASE-T1L, 10BASE-T1S, 100BASE-T1, and 1000BASE-T1. (See IEEE Std 802.3, Clause 96, ~~and~~ Clause 97, Clause 146, and Clause 147.)

[3]ISO publications are available from the International Organization for Standardization (http://www.iso.ch/). ISO publications are also available in the United States from the American National Standards Institute (http://www.ansi.org/).

[4]NAMUR publications are available from the User Association of Automation Technology in Process Industries (http://www.namur.net).

Change 1.4.198 as follows:

1.4.198 code-group: For IEEE 802.3, a set of encoded symbols representing encoded data or control information. For 100BASE-T4, a set of six ternary symbols that, when representing data, conveys an octet. For 100BASE-TX and 100BASE-FX, a set of five code-bits that, when representing data, conveys a nibble. For 100BASE-T2, a pair of PAM5×5 symbols that, when representing data, conveys a nibble. For 1000BASE-X, a set of ten bits that, when representing data, conveys an octet. For 1000BASE-T, a vector of four 8B1Q4 coded quinary symbols that, when representing data, conveys an octet. For 100BASE-T1, a set of ternary symbols that, when representing data, conveys three bits, as defined in 96.3. For 10BASE-T1L, a set of three ternary symbols that, when representing data, conveys a nibble, as defined in 146.3. (See IEEE Std 802.3, Clause 23, Clause 24, Clause 32, Clause 36, Clause 40, ~~and~~ Clause 96, and Clause 146.)

Change 1.4.319 as follows:

1.4.319 master Physical Layer (PHY): Within IEEE 802.3, in a 100BASE-T2 ~~or~~, 1000BASE-T, 10BASE-T1L, 100BASE-T1, 1000BASE-T1, or any MultiGBASE-T link containing a pair of PHYs, the PHY that uses an external clock for generating its clock signals to determine the timing of transmitter and receiver operations. It also uses the master transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link, or in the case of a PHY where Auto-Negotiation is optional and not used, master and slave PHY status is determined by management or hardware configuration. *See also:* **slave Physical Layer (PHY)**.

Insert the following new definition after 1.4.390 "physical header subframe (PHS)":

1.4.390a Physical Layer Collision Avoidance (PLCA): A method for generating transmit opportunities for 10BASE-T1S operating on mixing segments. (See IEEE Std 802.3, Clause 148.)

Change 1.4.456 as follows:

1.4.456 slave Physical Layer (PHY): Within IEEE 802.3, in a 100BASE-T2 ~~or~~, 1000BASE-T, 10BASE-T1L, 100BASE-T1, 1000BASE-T1, or any MultiGBASE-T link containing a pair of PHYs, the PHY that recovers its clock from the received signal and uses it to determine the timing of transmitter operations. It also uses the slave transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link, or in the case of a PHY where Auto-Negotiation is optional and not used, master and slave PHY status is determined by management or hardware configuration. *See also:* **master Physical Layer (PHY)**.

Change 1.4.471 as follows:

1.4.471 ternary symbol: In 10BASE-T1L, 100BASE-T4, and 100BASE-T1, a ternary data element. A ternary symbol can have one of three values: –1, 0, or +1. (See IEEE Std 802.3, Clause 23 ~~and~~, Clause 96, and Clause 146.)

Insert the following new definition after 1.4.495 "Type D PoDL System":

1.4.495a Type E PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 10BASE-T1L PHYs.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

DCR	direct current resistance
FSM	Finite State Machine
PLCA	Physical Layer Collision Avoidance

9. Repeater unit for 10 Mb/s baseband networks

9.1 Overview

Change the first paragraph of 9.1 as follows:

This clause specifies a repeater for use with IEEE 802.3 10 Mb/s baseband networks, with the exceptions of 10BASE-T1L (Clause 146) and 10BASE-T1S (Clause 147). A repeater for any other IEEE 802.3 network type is beyond the scope of this clause.

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

Change Figure 22-1 as follows (see changes at the bottom of the right column):

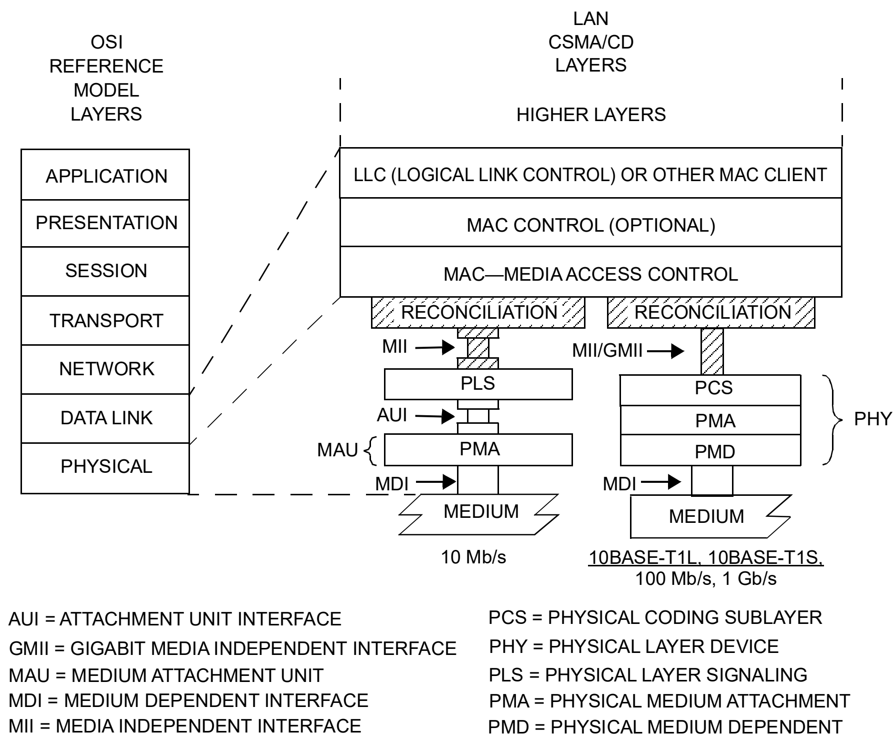


Figure 22–1—MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

22.2 Functional specifications

22.2.2 MII signal functional specifications

22.2.2.4 TXD (transmit data)

Change the second paragraph in 22.2.2.4 as follows:

For EEE capability, the RS shall use the combination of TX_EN deasserted, TX_ER asserted, and TXD<3:0> equal to 0001 as shown in Table 22–1 as a request to enter, or remain in a low power state.~~ Other values of TXD<3:0> with this combination of TX_EN and TX_ER shall have no effect upon the PHY.~~

Insert the following new paragraphs after the second paragraph in 22.2.2.4:

When PLCA capability is supported and enabled (see 30.16.1.1.1), the RS shall use the combination of TX_EN deasserted, TX_ER asserted, and TXD<3:0> equal to 0010 or 0011 as shown in Table 22–1 to send respectively a BEACON request or a COMMIT request as defined in 148.4.4.1.

When TX_EN is deasserted and TX_ER is asserted, values of TXD<3:0> other than 0001, 0010, and 0011 shall have no effect upon the PHY.

Change Table 22-1 as follows (unchanged rows not shown):

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
…			
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	~~0010~~0100 through 1111	Reserved
…			

22.2.2.5 TX_ER (transmit coding error)

Change the second paragraph in 22.2.2.5 as follows:

Assertion of the TX_ER signal shall not affect the transmission of data when TX_EN is deasserted. Additionally, the assertion of TX_ER signal shall not affect the transmission of data when a PHY is operating at 10 Mb/s~~, or when TX_EN is deasserted.~~ with the exception of 10BASE-T1L (see 146.3.3.1) and 10BASE-T1S (see 147.3.2.1, Figure 147–4).

22.2.2.8 RXD (receive data)

Insert the following new paragraph into 22.2.2.8 after the third paragraph ("For EEE capability, the PHY ...."):

When PLCA capability is supported and enabled, the PHY indicates that it is receiving a BEACON or COMMIT by asserting the RX_ER signal and driving respectively the values 0010 or 0011 onto RXD<3:0> while RX_DV is deasserted. See 148.4.4.1 for the definition and usage of PLCA BEACON and COMMIT.

Change Table 22-2 as follows (unchanged rows not shown):

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
…			
0	1	0010	PLCA BEACON indication
0	1	0011	PLCA COMMIT indication
0	1	~~0010~~0100 through 1101	Reserved
…			

22.8 Protocol implementation conformance statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[5]

22.8.2 Identification

22.8.2.3 Major capabilities/options

Insert the following new row at the end of the table in 22.8.2.3:

Item	Feature	Subclause	Status	Support	Value/Comment
*PLCA	Implementation of PLCA	22.2.2.4	O		

22.8.3 PICS proforma tables for reconciliation sublayer and media independent interface

22.8.3.2 MII signal functional specifications

Change the table in 22.8.3.2 as follows (unchanged rows not shown):

Item	Feature	Subclause	Status	Support	Value/Comment
…					
~~SF15~~	~~TXD<3:0> effect on PHY while TX_EN is de-asserted~~	~~22.2.2.4~~	~~M~~		~~No effect~~
…					
SF18	TX_ER effect on PHY while operating at 10 Mb/s (with the exception of 10BASE-T1S and 10BASE-T1L), or when TX_EN is deasserted	22.2.2.5	M		No effect on PHY
…					
SF39	Effect on PHY while TXD<3:0> is 0010, and TX_EN is deasserted, and TX_ER is asserted	22.2.2.4	PLCA: M		RS sends BEACON request
SF40	Effect on PHY while TXD<3:0> is 0011, and TX_EN is deasserted, and TX_ER is asserted	22.2.2.4	PLCA: M		RS sends COMMIT request
SF41	Effect on PHY while TXD<3:0> is any value other than 0010 or 0011, and TX_EN is deasserted, and TX_ER is asserted	22.2.2.4	PLCA: M		No effect

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

30. Management

30.2 Managed objects

30.2.2 Overview of managed objects

30.2.2.1 Text description of managed objects

Change the description for oPHYEntity in 30.2.2.1 as follows:

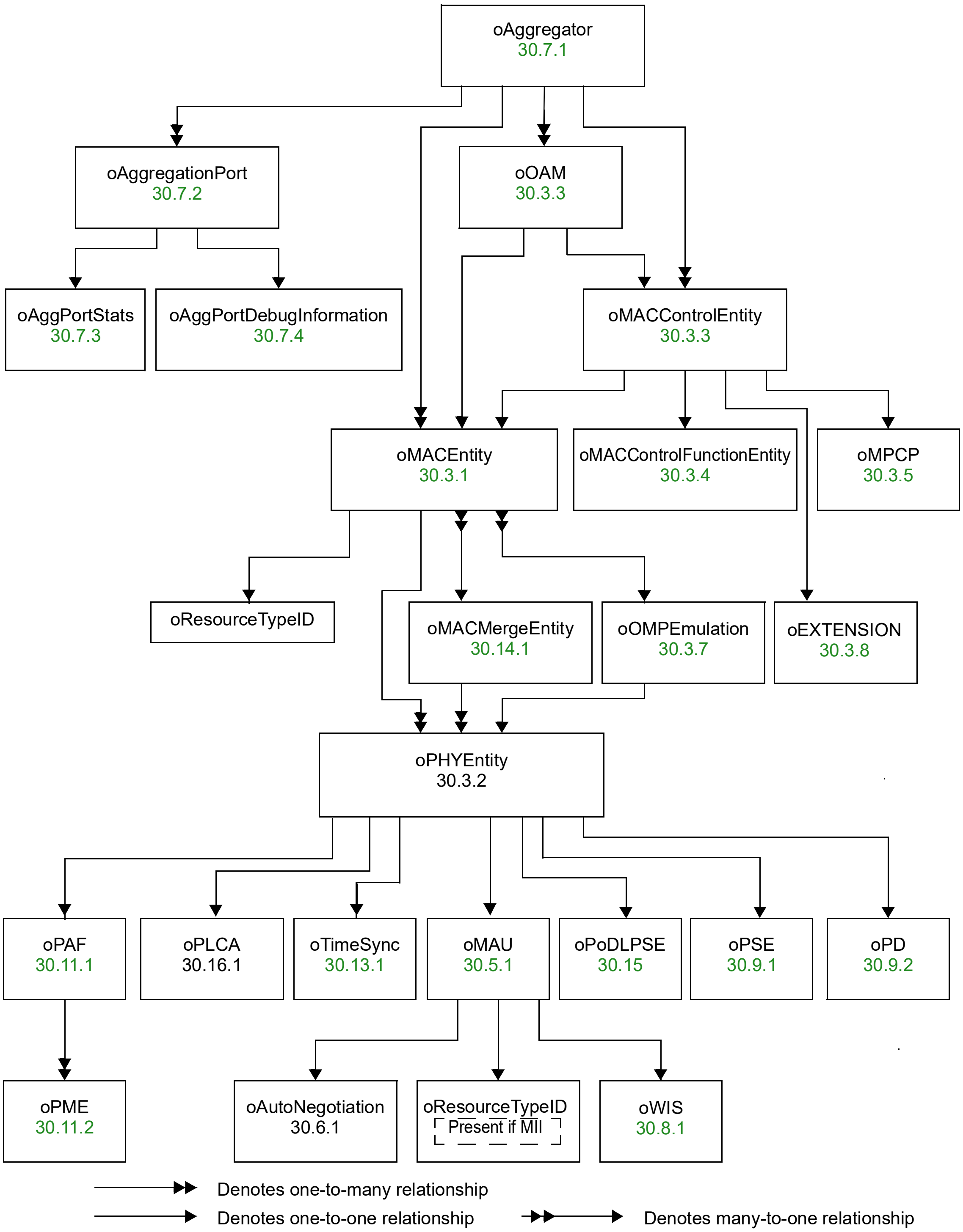
oPHYEntity	If oOMPEmulation is implemented, oPHYEntity is contained within oOMPEmulation. If oMACMergeEntity is implemented, oPHYEntity is contained within oMACMergeEntity. Otherwise oPHYEntity is contained within oMACEntity. Many instances of oPHYEntity may coexist within one instance of oMACEntity or oMACMergeEntity; however, only one PHY may be active for data transfer to and from the MAC at any one time. oPHYEntity is the managed object that contains the MAU, PAF, PLCA, PSE, and PoDLPSE managed objects in a DTE.

Insert the following description for oPLCA into 30.2.2.1 (as amended by IEEE Std 802.3bt-2018) after the description for oPAF:

oPLCA	If implemented, oPLCA is contained within oPHYEntity. The oPLCA managed object class provides the management controls necessary to allow an instance of a PLCA RS to be managed.

30.2.3 Containment

Replace Figure 30-3 with the following figure (which includes oPLCA):



NOTE—The objects oAggregator, oAggregationPort, oAggPortStats, and oAggPortDebugInformation are deprecated by IEEE Std 802.1AX™-2008.

Figure 30–3—DTE System entity relationship diagram

30.2.5 Capabilities

Change the last sentence of the first paragraph of 30.2.5 as follows:

The capabilities and packages for IEEE 802.3 Management are specified in Table 30-1a through ~~Table 30-10~~Table 30–11.

Insert the following new table (Table 30–11) after Table 30-10:

Table 30–11—PLCA capabilities

			PLCA capability (optional)
oPLCA managed object class (30.16.1)			
aPLCAAdminState	ATTRIBUTE	GET	X
aPLCAStatus	ATTRIBUTE	GET	X
aPLCABurstTimer	ATTRIBUTE	GET-SET	X
aPLCALocalNodeID	ATTRIBUTE	GET-SET	X
aPLCAMaxBurstCount	ATTRIBUTE	GET-SET	X
aPLCANodeCount	ATTRIBUTE	GET-SET	X
aPLCATransmitOpportunityTimer	ATTRIBUTE	GET-SET	X
acPLCAAdminControl	ACTION		X
acPLCAReset	ACTION		X

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "10 Mb/s":

10BASE-T1L Clause 146 10 Mb/s PAM3
10BASE-T1S Clause 147 10 Mb/s DME

30.3.2.1.3 aPhyTypeList

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "10 Mb/s":

10BASE-T1L Clause 146 10 Mb/s PAM3
10BASE-T1S Clause 147 10 Mb/s DME

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "10BASE-FLFD":

10BASE-T1L	Single balanced pair PHY as specified in Clause 146
10BASE-T1SHD	Single balanced pair PHY as specified in Clause 147, half duplex mode
10BASE-T1SMD	Single balanced pair PHY as specified in Clause 147, multidrop mode
10BASE-T1SFD	Single balanced pair PHY as specified in Clause 147, full duplex mode

30.5.1.1.4 aMediaAvailable

Change the fourth sentence of the third paragraph of the BEHAVIOUR DEFINED AS section of 30.5.1.1.4 as follows:

For <u>10BASE-T1L and </u>100BASE-T1, a link_status of OK maps to the enumeration "available".

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entries in APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "10BASE-T":

10BASE-T1L	10BASE-T1L as specified in Clause 146
10BASE-T1S	10BASE-T1S as specified in Clause 147

30.15 Layer management for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet

30.15.1 PoDL PSE managed object class

30.15.1.1 PoDL PSE attributes

30.15.1.1.4 aPoDLPSEType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.15.1.1.4 after the entry for "typeD":

typeE	Type E PoDL PSE

30.15.1.1.5 aPoDLPSEDetectedPDType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.15.1.1.5 after the entry for "typeD":

typeE	Type E PoDL PD

30.15.1.1.6 aPoDLPSEDetectedPDPowerClass

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.15.1.1.6 after the entry for "class 9":

class10	Class 10 PoDL PD
class11	Class 11 PoDL PD
class12	Class 12 PoDL PD
class13	Class 13 PoDL PD
class14	Class 14 PoDL PD
class15	Class 15 PoDL PD

Change text of BEHAVIOUR DEFINED AS section of 30.15.1.1.6 as shown:

BEHAVIOUR DEFINED AS:

A read-only value that indicates the class of the detected PoDL PD as specified in Table 104-1 and Table 104–1a. This value is only valid while a PD is being powered, that is the attribute aPoDLPSEPowerDetectionStatus is reporting the enumeration "deliveringPower".

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PD Class and PD Extended Class bits specified in 45.2.9.2.8 and 45.2.9.3.1a.;

Insert the following new subclauses (30.16 through 30.16.1.2.2) after 30.15 (and its subclauses):

30.16 Management for PLCA Reconciliation Sublayer

30.16.1 PLCA managed object class

This subclause formally defines the behaviours for the oPLCA managed object class attributes and actions.

30.16.1.1 PLCA attributes

30.16.1.1.1 aPLCAAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:
A read-only value that indicates the mode of operation of the Reconciliation Sublayer for PLCA operation. When PLCA is enabled, the Reconciliation Sublayer functions in PLCA mode, whose operation is defined by Clause 148. When PLCA functions are not supported or are disabled by the management interface (plca_en = FALSE), RS operation shall conform to the RS definition in Clause 22. By default, PLCA is disabled.;

30.16.1.1.2 aPLCAStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
TRUE
FALSE

BEHAVIOUR DEFINED AS:
A read-only value that indicates whether PLCA Control state diagram is receiving BEACON indication or transmitting BEACON request. This parameter maps to the plca_status variable in 148.4.6.2.;

30.16.1.1.3 aPLCANodeCount

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This value is assigned to define the number of nodes getting a transmit opportunity before a new BEACON is generated. Valid range is 0 to 255, inclusive. The default value is 8.;

30.16.1.1.4 aPLCALocalNodeID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This value is assigned to define the ID of the local node on the PLCA network. The default value is 255. Value range is 0 to 255, inclusive.;

30.16.1.1.5 aPLCATransmitOpportunityTimer

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This value is assigned to define the time between PLCA transmit opportunities for the node. aPLCATransmitOpportunityTimer maps to the duration of the timer to_timer. The value of aPLCATransmitOpportunityTimer represents the duration of to_timer in bit times. Valid range is 1 to 255, inclusive. The default value is 32. See 148.4.4.4.;

30.16.1.1.6 aPLCAMaxBurstCount

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
Maximum number of additional packets the node is allowed to transmit in a single transmit opportunity as specified in 148.4.4.1 and 148.4.4.2. Valid range is 0 to 255, inclusive. The default value is 0.;

30.16.1.1.7 aPLCABurstTimer

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This value sets the maximum number of bit-times PLCA waits for the MAC to send a new packet before yielding the transmit opportunity. See definition in 148.4.4.1 and 148.4.4.2. Valid range is 0 to 255, inclusive. The default value is 128.;

30.16.1.2 PLCA device actions

30.16.1.2.1 acPLCAAdminControl

ACTION

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPLCAAdminState. Setting acPLCAAdminControl to the disabled state sets the variable plca_en to FALSE and disables the PLCA functionality specified in Clause 148. Setting acPLCAAdminControl to the enabled state sets the variable plca_en to TRUE in Figure 148–3, Figure 148–4, Figure 148–5, Figure 148–6, and Figure 148–7.;

30.16.1.2.2 acPLCAReset

ACTION

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
reset
normal

BEHAVIOUR DEFINED AS:

This action provides a means to reset the PLCA Reconciliation Sublayer functions. See 148.4.4.2.;

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.2103 through 1.2293~~303~~	Reserved	
1.2294	10BASE-T1L PMA control	45.2.1.186a
1.2295	10BASE-T1L PMA status	45.2.1.186b
1.2296	10BASE-T1L test mode control	45.2.1.186c
1.2297	10BASE-T1S PMA control	45.2.1.186d
1.2298	10BASE-T1S PMA status	45.2.1.186e
1.2299	10BASE-T1S test mode control	45.2.1.186f
1.2300 through 1.2303	Reserved	
…		

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert the following new row at the beginning of Table 45–9:

Table 45–9—Transmit fault description location

PMA/PMD	Description location
10BASE-T1L	146.4.2

45.2.1.7.5 Receive fault (1.8.10)

Insert the following new row at the beginning of Table 45–10:

Table 45–10—Receive fault description location

PMA/PMD	Description location
10BASE-T1L	146.4.3

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

Change Table 45-19 as follows (unchanged rows not shown):

Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:~~2~~4	Reserved	Value always 0	RO
1.18.3	10BASE-T1S ability	1 = PMA/PMD is able to perform 10BASE-T1S 0 = PMA/PMD is not able to perform 10BASE-T1S	RO
1.18.2	10BASE-T1L ability	1 = PMA/PMD is able to perform 10BASE-T1L 0 = PMA/PMD is not able to perform 10BASE-T1L	RO
…			

[a]RO = Read only

45.2.1.185 BASE-T1 PMA/PMD control register (Register 1.2100)

Change Table 45-149 as follows (unchanged rows not shown):

Table 45–149—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.3:0	Type Selection	3 2 1 0 1 x x x = Reserved 0 1 x x = Reserved 0 0 1 1 = 10BASE-T1S 0 0 1 ~~x~~0 = ~~Reserved~~10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.185.2 Type selection (1.2100.3:0)

Change 45.1.185.2 as follows:

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. When these bits are set to 0000, the mode of operation is 100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. When these bits are set to 0010, the mode of operation is 10BASE-T1L. When these bits are set to 0011, the mode of operation is 10BASE-T1S. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

Insert the following new subclauses (45.2.1.186a through 45.2.1.186f.1, including Table 45-150a through Table 45-150f) after 45.2.1.186.1:

45.2.1.186a 10BASE-T1L PMA control register (Register 1.2294)

The assignment of bits in the 10BASE-T1L PMA control register is shown in Table 45–150a.

Table 45–150a—10BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2294.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2294.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2294.13	Reserved	Value always zero	RO
1.2294.12	Transmit voltage amplitude control	1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode	R/W
1.2294.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2294.10	EEE enable	1 = Enable EEE mode 0 = Disable EEE mode	R/W
1.2294.9:1	Reserved	Value always 0	RO
1.2294.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.186a.1 PMA reset (1.2294.15)

Resetting the 10BASE-T1L PMA is accomplished by setting bit 1.2294.15 to one. This action shall set all 10BASE-T1L PMA registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1L PMA and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1L PMA shall return a value of one in bit 1.2294.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PMA is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2294.15.

During a reset, the 10BASE-T1L PMA shall respond to reads from bits 1.2294.15, 1.8.15:14, and 1.0.15. Reads for all other bits are indeterminate, and the values are invalid.

NOTE—This operation may interrupt data communication.

Bit 1.2294.15 is a copy of bit 1.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PMA.

45.2.1.186a.2 Transmit disable (1.2294.14)

When bit 1.2294.14 is set to one, the PMA shall disable output on the transmit path. When bit 1.2294.14 is set to zero, the PMA shall enable output on the transmit path.

Bit 1.2294.14 is a copy of bit 1.9.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.186a.3 Transmit voltage amplitude control (1.2294.12)

Bit 1.2294.12 is used to set the 2.4 Vpp operating mode when Auto-Negotiation enable bit 7.512.12 is set to zero or if Auto-Negotiation is not implemented. If bit 1.2294.12 is set to one, the PHY shall operate in 2.4 Vpp operating mode according to 146.5.4.1. If bit 1.2294.12 is set to zero, the PHY shall operate in 1.0 Vpp operating mode according to 146.5.4.1. The default value of bit 1.2294.12 is zero. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.186a.4 Low-power (1.2294.11)

When the low-power ability is supported, the 10BASE-T1L PMA may be placed into a low-power mode by setting bit 1.2294.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1L PMA. The behavior of the 10BASE-T1L PMA in transition to and from the low-power mode is implementation specific, and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2294.11 is zero.

NOTE—This operation may interrupt data communication. The data path of the 10BASE-T1L PMA, depending on implementation, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2294.11 is a copy of bit 1.0.11, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1L PMA in low-power mode.

45.2.1.186a.5 EEE enable (1.2294.10)

Bit 1.2294.10 is used to enable EEE functionality when Auto-Negotiation enable bit 7.512.12 is set to zero or if Auto-Negotiation is not implemented. If bit 1.2294.10 is set to one, the PHY shall operate with EEE enabled. If bit 1.2294.10 is set to zero, the PHY shall operate with EEE disabled. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one. The default value of bit 1.2294.10 is zero.

45.2.1.186a.6 Loopback (1.2294.0)

The 10BASE-T1L PMA shall be placed in near-end loopback mode of operation when bit 1.2294.0 is set to one. When in loopback mode, the 10BASE-T1L PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2294.0 is zero. Bit 1.2294.0 is a copy of 1.0.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.1.186b 10BASE-T1L PMA status register (Register 1.2295)

The assignment of bits in the 10BASE-T1L PMA status register is shown in Table 45–150b.

Table 45–150b—10BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2295.15:14	Reserved	Value always 0	RO
1.2295.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2295.12	2.4 Vpp operating mode ability	1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability	RO
1.2295.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2295.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2295.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2295.8:3	Reserved	Value always 0	RO
1.2295.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2295.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2295.0	Receive link status	1 = PMA receive link up 0 = PMA receive link down	RO/LL

[a]RO = Read only, LL = Latching low, LH = Latching high

45.2.1.186b.1 Loopback ability (1.2295.13)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports PMA loopback. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support PMA loopback.

45.2.1.186b.2 2.4 Vpp operating mode ability (1.2295.12)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports a transmit level of 2.4 Vpp. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support a transmit level of 2.4 Vpp.

45.2.1.186b.3 Low-power ability (1.2295.11)

When read as a one, bit 1.2295.11 indicates that the 10BASE-T1L PMA supports the low-power ability. When read as a zero, bit 1.2295.11 indicates that the 10BASE-T1L PMA does not support the low-power ability. If the 10BASE-T1L PMA supports the low-power ability, then it is controlled using either bit 1.2294.11 or bit 1.0.11.

45.2.1.186b.4 EEE ability (1.2295.10)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports EEE. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support EEE.

45.2.1.186b.5 Receive fault ability (1.2295.9)

When read as a one, bit 1.2295.9 indicates that the 10BASE-T1L PMA has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2295.9 indicates that the 10BASE-T1L PMA does not have the ability to detect a fault condition on the receive path.

45.2.1.186b.6 Receive polarity (1.2295.2)

When read as a zero, bit 1.2295.2 indicates that the polarity of the receiver is not reversed. When read as a one, bit 1.2295.2 indicates that the polarity of the receiver is reversed.

45.2.1.186b.7 Receive fault (1.2295.1)

When read as a one, bit 1.2295.1 indicates that the 10BASE-T1L PMA has detected a fault condition on the receive path. When read as a zero, bit 1.2295.1 indicates that the 10BASE-T1L PMA has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional, and the ability to detect such a condition is advertised by bit 1.2295.9. The 10BASE-T1L PMA that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The receive fault bit shall be implemented with latching high behavior.

45.2.1.186b.8 Receive link status (1.2295.0)

When read as a one, bit 1.2295.0 indicates that the 10BASE-T1L PMA receive link is up. When read as a zero, bit 1.2295.0 indicates that the 10BASE-T1L PMA receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.186c 10BASE-T1L test mode control register (Register 1.2296)

The assignment of bits in the 10BASE-T1L test mode control register is shown in Table 45–150c. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–150c—10BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2296.15:13	Test mode control	15 14 13 1 x x = Reserved 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2296.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.1.186c.1 Test mode control (1.2296.15:13)

Transmitter test mode operations defined by bits 1.2296.15:13 are described in 146.5.2. The default value for bits 1.2296.15:13 is zero.

45.2.1.186d 10BASE-T1S PMA control register (Register 1.2297)

The assignment of bits in the 10BASE-T1S PMA control register is shown in Table 45–150d.

Table 45–150d—10BASE-T1S PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2297.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2297.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2297.13:12	Reserved	Value always 0	RO
1.2297.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2297.10	Multidrop mode	1 = Enable operation over mixing segment network 0 = Disable operation over mixing segment network	R/W
1.2297.9:1	Reserved	Value always 0	RO
1.2297.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.186d.1 PMA reset (1.2297.15)

Resetting the 10BASE-T1S PMA is accomplished by setting bit 1.2297.15 to one. This action shall set all 10BASE-T1S PMA registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PMA and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1S PMA shall return a value of one in bit 1.2297.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PMA is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2297.15.

During a reset, the 10BASE-T1S PMA shall respond to reads from bits 1.2297.15, 1.8.15:14, and 1.0.15. All other register bits should be ignored.

NOTE—This operation may interrupt communication.

Bit 1.2297.15 is a copy of 1.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1S PMA.

45.2.1.186d.2 Transmit disable (1.2297.14)

When bit 1.2297.14 is set to one, the PMA shall disable output on the transmit path. When bit 1.2297.14 is set to zero, the PMA shall enable output on the transmit path.

Bit 1.2297.14 is a copy of bit 1.9.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.186d.3 Low-power (1.2297.11)

When the low-power ability is supported, the 10BASE-T1S PMA may be placed into a low-power mode by setting bit 1.2297.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1S PMA. The behavior of the 10BASE-T1S PMA in transition to and from the low-power mode is implementation specific, and any interface signals should not be relied upon. While in the low-power mode, the device shall respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2297.11 is zero.

NOTE—The time from low-power mode to full operation is implementation specific.

Bit 1.2297.11 is a copy of bit 1.0.11, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1S PMA in low-power mode.

45.2.1.186d.4 Multidrop mode (1.2297.10)

When Auto-Negotiation is implemented and enabled, writing to this bit shall have no effect on the PHY, and the PCS multidrop variable shall be set to FALSE. If multidrop mode is not supported according to bit 1.2298.10, then writing to bit 1.2297.10 shall have no effect, and the multidrop variable shall be set to FALSE. Otherwise, if bit 1.2297.10 is set to one, the 10BASE-T1S PMA shall operate in multidrop mode, and the multidrop variable is set to TRUE; and if bit 1.2297.10 is set to zero, the multidrop variable is set to FALSE. If multidrop mode is supported according to bit 1.2298.10, then the default value of bit 1.2297.10 should be one.

45.2.1.186d.5 Loopback (1.2297.0)

The 10BASE-T1S PMA shall be placed in loopback mode of operation when loopback bit 1.2297.0 is set to one. When in loopback mode, the 10BASE-T1S PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2297.0 is zero. Bit 1.2297.0 is a copy of 1.0.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.1.186e 10BASE-T1S PMA status register (Register 1.2298)

The assignment of bits in the 10BASE-T1S PMA status register is shown in Table 45–150e.

Table 45–150e—10BASE-T1S PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2298.15:14	Reserved	Value always 0	RO
1.2298.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO

Table 45–150e—10BASE-T1S PMA status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.2298.12	Reserved	Value always 0	RO
1.2298.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2298.10	Multidrop mode ability	1 = PMA has the ability to operate over a mixing segment network 0 = PMA does not have the ability to operate over a mixing segment network	RO
1.2298.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2298.8:2	Reserved	Value always 0	RO
1.2298.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2298.0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.1.186e.1 10BASE-T1S loopback ability (1.2298.13)

When read as a one, this bit indicates that the 10BASE-T1S PHY supports PMA loopback. When read as a zero, this bit indicates that the 10BASE-T1S PHY does not support PMA loopback.

45.2.1.186e.2 Low-power ability (1.2298.11)

When read as a one, bit 1.2298.11 indicates that the 10BASE-T1S PMA supports the low-power ability. When read as a zero, bit 1.2298.11 indicates that the 10BASE-T1S PMA does not support the low-power feature. If the 10BASE-T1S PMA supports the low-power feature, then it is controlled using either bit 1.2297.11 or bit 1.0.11.

45.2.1.186e.3 Multidrop ability (1.2298.10)

When read as a one, bit 1.2298.10 indicates that the 10BASE-T1S PMA supports multidrop mode (see Clause 147). When read as a zero, bit 1.2298.10 indicates that the 10BASE-T1S PMA does not support multidrop mode. If the 10BASE-T1S PMA supports multidrop mode, then it is controlled using bit 1.2297.10; otherwise, bit 1.2297.10 has no effect.

45.2.1.186e.4 Receive fault ability (1.2298.9)

When read as a one, bit 1.2298.9 indicates that the 10BASE-T1S PMA has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2298.9 indicates that the 10BASE-T1S PMA does not have the ability to detect a fault condition on the receive path.

45.2.1.186e.5 Receive fault (1.2298.1)

When read as a one, bit 1.2298.1 indicates that the 10BASE-T1S PMA has detected a fault condition on the receive path. When read as a zero, bit 1.2298.1 indicates that the 10BASE-T1S PMA has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional, and the ability to detect such a condition is advertised by bit 1.2298.9. The 10BASE-T1S PMA that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. This bit shall be implemented with latching high behavior.

45.2.1.186f 10BASE-T1S test mode control register (Register 1.2299)

The assignment of bits in the 10BASE-T1S test mode control register is shown in Table 45–150f. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–150f—10BASE-T1S test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2299.15:13	Test mode control	15 14 13 1 1 x = Reserved 1 0 1 = Reserved 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2299.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.1.186f.1 Test mode control (1.2299.15:13)

Transmitter test mode operations defined by bits 1.2299.15:13 are described in 147.5.2. The default value for bits 1.2299.15:13 is zero.

45.2.3 PCS registers

Change Table 45–176 as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
…		
3.1809 through 3.~~2303~~2277	Reserved	
3.2278	10BASE-T1L PCS control	45.2.3.68a
3.2279	10BASE-T1L PCS status	45.2.3.68b
3.2280 through 3.2290	Reserved	

Table 45–176—PCS registers *(continued)*

Register address	Register name	Subclause
3.2291	10BASE-T1S PCS control	45.2.3.68c
3.2292	10BASE-T1S PCS status	45.2.3.68d
3.2293	10BASE-T1S PCS diagnostic 1	45.2.3.68e
3.2294	10BASE-T1S PCS diagnostic 2	45.2.3.68f
3.2295 through 3.2303	Reserved	
…		

Insert the following new subclauses (45.2.3.68a through 45.2.3.68f.1, including Table 45-237a through Table 45-237f) after 45.2.3.68:

45.2.3.68a 10BASE-T1L PCS control register (Register 3.2278)

The assignment of bits in the 10BASE-T1L PCS control register is shown in Table 45–237a. The default value for each bit of the 10BASE-T1L PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–237a—10BASE-T1L PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2278.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2278.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2278.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.68a.1 PCS reset (3.2278.15)

Resetting the 10BASE-T1L PCS is accomplished by setting bit 3.2278.15 to one. This action shall set all 10BASE-T1L PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1L PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1L PCS shall return a value of one in bit 3.2278.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2278.15. During a reset, a PCS shall respond to reads from bits 3.0.15, 3.8.15:14, and 3.2278.15. Reads for all other bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2278.15 is a copy of 3.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PCS.

45.2.3.68a.2 Loopback (3.2278.14)

The 10BASE-T1L PCS shall be placed in a loopback mode of operation when bit 3.2278.14 is set to one. When in loopback mode, the 10BASE-T1L PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2278.14 is zero.

Bit 3.2278.14 is a copy of 3.0.14, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.68b 10BASE-T1L PCS status register (Register 3.2279)

The assignment of bits in the 10BASE-T1L PCS status register is shown in Table 45–237b. All the bits in the 10BASE-T1L PCS status register are read only; a write to the 10BASE-T1L PCS status register shall have no effect.

Table 45–237b—10BASE-T1L PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2279.15:12	Reserved	Value always 0	RO
3.2279.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH
3.2279.6:3	Reserved	Value always 0	RO
3.2279.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2279.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.68b.1 Tx LPI received (3.2279.11)

When read as a one, bit 3.2279.11 indicates that the transmit 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.11 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.68b.2 Rx LPI received (3.2279.10)

When read as a one, bit 3.2279.10 indicates that the receive 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.10 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.68b.3 Tx LPI indication (3.2279.9)

When read as a one, bit 3.2279.9 indicates that the transmit 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.9 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.68b.4 Rx LPI indication (3.2279.8)

When read as a one, bit 3.2279.8 indicates that the receive 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.8 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.68b.5 Fault (3.2279.7)

When read as a one, bit 3.2279.7 indicates that the 10BASE-T1L PCS has detected a fault condition on either the transmit or receive path. When read as a zero, bit 3.2279.7 indicates that the 10BASE-T1L PCS has not detected a fault condition. This bit shall be implemented with latching high behavior.

45.2.3.68b.6 PCS receive link status (3.2279.2)

When read as a one, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link is up. When read as a zero, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link was down since the last read from this bit. This bit shall be implemented with latching low behavior and is a reflection of the variable scr_status. If the bit is read while scr_status = OK, then this bit is set. If scr_status = NOT_OK, then this bit is reset.

45.2.3.68c 10BASE-T1S PCS control register (Register 3.2291)

The assignment of bits in the 10BASE-T1S PCS control register is shown in Table 45–237c. The default value for each bit of the 10BASE-T1S PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–237c—10BASE-T1S PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2291.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2291.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2291.13:9	Reserved	Value always 0	RO
3.2291.8	Duplex mode	1 = Set to half duplex 0 = Set to full duplex	R/W
3.2291.7:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.68c.1 PCS reset (3.2291.15)

Resetting the 10BASE-T1S PCS is accomplished by setting bit 3.2291.15 to one. This action shall set all 10BASE-T1S PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1S PCS shall return a value of one in bit 3.2291.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2291.15. During a reset, a PCS shall respond to reads from bits 3.0.15, 3.8.15:14, and 3.2291.15. Reads for all other bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2291.15 is a copy of 3.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1S PCS.

45.2.3.68c.2 Loopback (3.2291.14)

The 10BASE-T1S PCS shall be placed in a loopback mode of operation when bit 3.2291.14 is set to one. When in loopback mode, the 10BASE-T1S PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2291.14 is zero.

Bit 3.2291.14 is a copy of 3.0.14, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.68c.3 Duplex mode (3.2291.8)

Bit 3.2291.8 is used to configure the PCS duplex_mode variable when not operating in Multidrop mode and when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. If bit 3.2291.8 is set to one, then duplex_mode is set to DUPLEX_HALF. If bit 3.2291.8 is set to zero, then duplex_mode is set to DUPLEX_FULL. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

Bit 3.2291.8 is a copy of bit 0.8 (see Table 22–7), and setting or clearing either bit shall set or clear the other bit.

45.2.3.68d 10BASE-T1S PCS status register (Register 3.2292)

The assignment of bits in the 10BASE-T1S PCS status register is shown in Table 45–237d. All the bits in the 10BASE-T1S PCS status register are read only; a write to the 10BASE-T1S PCS status register shall have no effect.

Table 45–237d—10BASE-T1S PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2292.15:8	Reserved	Value always 0	RO
3.2292.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH
3.2292.6:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.3.68d.1 Fault (3.2292.7)

When read as a one, bit 3.2292.7 indicates that the 10BASE-T1S PCS has detected a fault condition on either the transmit or receive path. When read as a zero, bit 3.2292.7 indicates that the 10BASE-T1S PCS has not detected a fault condition. This bit shall be implemented with latching high behavior.

45.2.3.68e 10BASE-T1S PCS diagnostic 1 (Register 3.2293)

The assignment of bits in the 10BASE-T1S PCS diagnostic 1 register is shown in Table 45–237e. All the bits in the 10BASE-T1S PCS diagnostic 1 register are read only and self-clear on read; a write to the 10BASE-T1S PCS diagnostic 1 register shall have no effect.

Table 45–237e—10BASE-T1S PCS diagnostic 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2293.15:0	Remote jabber count	16-bit field counting the number of remote jabber errors received since last read of this register	RO, SC

[a]RO = Read only, SC = Self-clearing

45.2.3.68e.1 Remote jabber count (3.2293.15:0)

Bits 3.2293.15:0 report the number of received jabber events since the last time register 3.2293 was read. The remote jabber count shall not wrap. When the maximum allowed value (65 535) is reached, the count stops until this register is cleared by a read operation.

45.2.3.68f 10BASE-T1S PCS diagnostic 2 (Register 3.2294)

The assignment of bits in the 10BASE-T1S PCS diagnostic 2 register is shown in Table 45–237f. All the bits in the 10BASE-T1S PCS diagnostic 2 register are read only and self-clear on read; a write to the 10BASE-T1S PCS diagnostic 2 register shall have no effect.

Table 45–237f—10BASE-T1S PCS diagnostic 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2294.15:0	CorruptedTxCnt	16-bit field counting each time a transmission initiated locally results in a corrupted signal at the MDI since last read of this register	RO, SC

[a]RO = Read only, SC = Self-clearing

45.2.3.68f.1 CorruptedTxCnt (3.2294.15:0)

Bits 3.2294.15:0 count up at each positive edge of the MII signal COL. When the maximum allowed value (65 535) is reached, the count stops until this register is cleared by a read operation.

45.2.7 Auto-Negotiation registers

Change Table 45–309 as follows (unchanged rows not shown):

Table 45–309—Auto-Negotiation MMD registers

Register address	Register name	Subclause
…		
7.526	10BASE-T1 AN control	45.2.7.25
7.527	10BASE-T1 AN status	45.2.7.26
7.52~~6~~8 through 7.32767	Reserved	
…		

Insert the following new subclauses (45.2.7.25 and 45.2.7.26, including Table 45–330a and Table 45–330b) after 45.27.24:

45.2.7.25 10BASE-T1 AN control register (Register 7.526)

The assignment of bits in the 10BASE-T1 AN control register is shown in Table 45–330a. The default value for each bit of the 10BASE-T1 AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–330a—10BASE-T1 AN control register bit definitions

Bit(s)	Name	Description	R/W[a]
7.526.15	10BASE-T1L capability advertisement	1 = Advertise PHY as 10BASE-T1L capable 0 = Do not advertise PHY as 10BASE-T1L capable	R/W
7.526.14	10BASE-T1L EEE ability advertisement	1 = Advertise that the 10BASE-T1L PHY has EEE ability 0 = Do not advertise that the 10BASE-T1L PHY has EEE ability (default)	R/W
7.526.13	10BASE-T1L increased transmit/ receive level ability advertisement	1 = Advertise that the 10BASE-T1L PHY has increased transmit/receive level ability 0 = Do not advertise that the 10BASE-T1L PHY has increased transmit/receive level ability (default)	R/W
7.526.12	10BASE-T1L increased transmit level request	1 = Request 10BASE-T1L increased transmit level 0 = Do not request 10BASE-T1L increased transmit level (default)	R/W
7.526.11:8	Reserved	Value always 0	RO
7.526.7	10BASE-T1S full duplex ability advertisement	1 = Advertise that the 10BASE-T1S PHY has full duplex ability 0 = Do not advertise that the 10BASE-T1S PHY has full duplex ability	R/W
7.526.6	10BASE-T1S half duplex capability advertisement	1 = Advertise PHY as 10BASE-T1S half duplex capable 0 = Do not advertise PHY as 10BASE-T1S half duplex capable	R/W
7.526.5:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.7.25.1 10BASE-T1L capability advertisement (7.526.15)

Bit 7.526.15 is used to select whether Auto-Negotiation advertises the capability to operate as a 10BASE-T1L PHY. If bit 7.526.15 is set to one, the PHY shall advertise 10BASE-T1L capability. If bit 7.526.15 is set to zero, the PHY shall not advertise the capability to operate as a 10BASE-T1L PHY.

45.2.7.25.2 10BASE-T1L EEE ability advertisement (7.526.14)

If the device supports EEE ability for 10BASE-T1L, as defined in 146.1.2.3, and EEE operation is desired, bit 7.526.14 shall be set to one.

45.2.7.25.3 10BASE-T1L increased transmit/receive level ability advertisement (7.526.13)

If the device supports the 2.4 Vpp operating mode for 10BASE-T1L, as defined in 146.5.4.1, bit 7.526.13 shall be set to one.

45.2.7.25.4 10BASE-T1L increased transmit level request (7.526.12)

If the device supports the 2.4 Vpp operating mode for 10BASE-T1L, as defined in 146.5.4.1, and the 2.4 Vpp transmit voltage operation is desired, bit 7.526.12 is set to one. Bit 7.526.12 is used to select whether Auto-Negotiation advertises a request to operate the 10BASE-T1L PHY in increased transmit level mode. If bit 7.526.12 is set to one, the PHY shall advertise a request to operate the 10BASE-T1L PHY in increased transmit level mode. If bit 7.526.12 is set to zero, the PHY shall not advertise a request to operate the 10BASE-T1L PHY in increased transmit level mode.

45.2.7.25.5 10BASE-T1S full duplex ability advertisement (7.526.7)

Bit 7.526.7 is used to select whether Auto-Negotiation advertises the ability to operate the 10BASE-T1S PHY in full duplex mode. If bit 7.526.7 is set to one, the PHY shall advertise 10BASE-T1S full duplex capability. If bit 7.526.7 is set to zero, the PHY shall not advertise the ability to operate in 10BASE-T1S full duplex mode.

45.2.7.25.6 10BASE-T1S half duplex capability advertisement (7.526.6)

Bit 7.526.6 is used to select whether Auto-Negotiation advertises the capability to operate the 10BASE-T1S PHY in half duplex mode. If bit 7.526.6 is set to one, the PHY shall advertise 10BASE-T1S half duplex capability. If bit 7.526.6 is set to zero, the PHY shall not advertise the capability to operate in 10BASE-T1S half duplex mode.

45.2.7.26 10BASE-T1 AN status register (Register 7.527)

The assignment of bits in the 10BASE-T1 AN status register is shown in Table 45–330b. All the bits in the 10BASE-T1 AN status register are read only; therefore, a write to the 10BASE-T1 AN status register shall have no effect.

When the AN process has been completed, this register shall reflect the contents of the link partner's 10BASE-T1 AN control register. The definitions for the contents of the 10BASE-T1 AN status register are given by the definitions for the contents on the link partner's 10BASE-T1 control register, 7.526 (see 45.2.7.25).

Table 45–330b—10BASE-T1 AN status register bit definitions

Bit(s)	Name	Description	R/W[a]
7.527.15	10BASE-T1L link partner capability advertisement	1 = Link partner is advertising PHY as 10BASE-T1L capable 0 = Link partner is not advertising PHY as 10BASE-T1L capable	RO
7.527.14	10BASE-T1L link partner EEE ability advertisement	1 = Link partner is advertising that the 10BASE-T1L PHY has EEE ability 0 = Link partner is not advertising that the 10BASE-T1L PHY has EEE ability	RO
7.527.13	10BASE-T1L link partner increased transmit/receive level ability advertisement	1 = Link partner is advertising that the 10BASE-T1L PHY has increased transmit/ receive level ability 0 = Link partner is not advertising that the 10BASE-T1L PHY has increased transmit/ receive level ability	RO

Table 45–330b—10BASE-T1 AN status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
7.527.12	10BASE-T1L link partner increased transmit level request	1 = Link partner is requesting 10BASE-T1L link partner increased transmit level 0 = Link partner is not requesting 10BASE-T1L link partner increased transmit level	RO
7.527.11:8	Reserved	Value always 0	RO
7.527.7	10BASE-T1S link partner full duplex ability advertisement	1 = Link partner is advertising that the 10BASE-T1S PHY has full duplex ability 0 = Link partner is not advertising that the 10BASE-T1S PHY has full duplex ability	RO
7.527.6	10BASE-T1S link partner half duplex capability advertisement	1 = Link partner is advertising PHY as 10BASE-T1S half duplex capable 0 = Link partner is not advertising PHY as 10BASE-T1S half duplex capable	RO
7.527.5:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.9 Power Unit Registers

Insert the following new rows at the end of Table 45-338:

Table 45–338—Power Unit MMD Registers

Register address	Register name	Subclause
13.3	PoDL PSE Status 3	45.2.9.4
13.4	PoDL PSE Status 4	45.2.9.5

45.2.9.1 PoDL PSE Control register (Register 13.0)

Change Table 45–339 as follows (unchanged rows not shown):

Table 45–339—PoDL PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
13.0.15:~~2~~3	Reserved	Value always 0	RO
13.0.2	Enable cable resistance measurement	1 = Cable resistance measurement enabled 0 = Cable resistance measurement disabled	R/W
…			

[a]R/W = Read/Write, RO = Read only

45.2.9.2 PoDL PSE Status 1 register (Register 13.1)

Change Table 45–340 as follows (unchanged rows not shown):

Table 45–340—PoDL PSE Status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
13.1.9:7	PSE Type	9 8 7 1 ~~x~~1 x = Reserved 1 0 1 = Reserved 1 0 0 = Type E PSE 0 1 1 = Type D PSE 0 1 0 = Type C PSE 0 0 1 = Type B PSE 0 0 0 = Type A PSE	RO
13.1.6:3	PD Class	6 5 4 3 1 1 ~~x~~1 ~~x~~1 = ~~Reserved~~Extend to PoDL PSE status 2 register 1 1 1 0 = Class code 14 1 1 0 1 = Class code 13 1 1 0 0 = Class code 12 1 0 1 ~~x~~1 = ~~Reserved~~Class code 11 1 0 1 0 = Class code 10 1 0 0 1 = Class code 9 1 0 0 0 = Class code 8 0 1 1 1 = Class code 7 0 1 1 0 = Class code 6 0 1 0 1 = Class code 5 0 1 0 0 = Class code 4 0 0 1 1 = Class code 3 0 0 1 0 = Class code 2 0 0 0 1 = Class code 1 0 0 0 0 = Class code 0	RO
…			

[a]RO = Read only, LH = Latching high

45.2.9.2.7 PSE Type (13.1.9:7)

Change 45.2.9.2.7 as follows:

Bits 13.1.9:7 report the PSE Type of the PSE as specified in 104.4.1. When read as 000, bits 13.1.9:7 indicate a Type A PSE;~~,~~ when read as 001, a Type B PSE is indicated;~~,~~ ~~and~~ when read as 010, a Type C PSE is indicated;~~.~~ ~~and~~ when read as 011, a Type D PSE is indicated; and when read as 100, a Type E PSE is indicated. Values of 101 and 11x ~~1xx~~ are reserved.

45.2.9.2.8 PD Class (13.1.6:3)

Change the last sentence of 45.2.9.2.8 as follows:

When read as 0000, a Class 0 PD is indicated;~~,~~ when read as 0001, a Class 1 PD is indicated;~~,~~ when read as 0010, a Class 2 PD is indicated;~~,~~ when read as 0011, a Class 3 PD is indicated;~~,~~ when read as 0100, a Class 4 PD is indicated;~~,~~ when read as 0101, a Class 5 PD is indicated;~~,~~ when read as 0110, a Class 6 PD is indicated;, when read as 0111, a Class 7 PD is indicated;, when read as 1000, a Class 8 PD is indicated;, and when read as 1001, a Class 9 PD is indicated.; when read as 1010, a Class 10 PD is indicated; when read as 1011, a Class 11 PD is indicated; when read as 1100, a Class 12 PD is indicated; when read as 1101, a Class 13 PD is indicated; when read as 1110, a Class 14 PD is indicated; and when read as 1111, the Class is indicated by the PD Extended Class (13.2.10:9) bits.

45.2.9.3 PoDL PSE Status 2 register (Register 13.2)

Change Table 45–341 as follows (unchanged rows not shown):

Table 45–341—PoDL PSE Status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
13.2.14:311	Reserved	Value always 0	RO
13:2.10:9	PD Extended Class	10 9 1 1 = Reserved 1 0 = Reserved 0 1 = Reserved 0 0 = Class code 15	RO
13.2.8:3	Reserved	Value always 0	RO
13.2.2:0	PD Type	2 1 0 1 1 1 = Unknown 1 1 0 = Reserved 1 0 x1 = Reserved 1 0 0 = Type E PD 0 1 1 = Type D PD 0 1 0 = Type C PD 0 0 1 = Type B PD 0 0 0 = Type A PD	RO

[a]RO = Read only, LH = Latching high

Insert the following new subclause (45.2.9.3.1a) after 45.2.9.3.1:

45.2.9.3.1a PD Extended Class (13.2.10:9)

When bits 13.2.10:9 are read as 00, a Class 15 PD is indicated. Values of 01 and 1x are reserved.

45.2.9.3.2 PD Type (13.2.2:0)

Change the last two sentences of 45.2.9.3.2 as follows:

When read as 000, bits 13.2.2:0 indicate a Type A PD; when read as 001, a Type B PD is indicated; when read as 010, a Type C PD is indicated; and when read as 011, a Type D PD is indicated; and when read as 100, a Type E PD is indicated. Values of 101x and 110 are reserved.

Insert the following new subclauses (45.2.9.4 through 45.2.9.5.1, including Table 45-341a and Table 45-341b) after 45.2.9.3.2:

45.2.9.4 PoDL PSE Status 3 register (Register 13.3)

The PoDL PSE Status 3 Register is defined if cable resistance measurement is supported.

Table 45–341a—PoDL PSE Status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.3.15:12	Reserved	Value always zero	RO
13.3.11:0	PD Assigned Power	PD Assigned Power, 0.025 W per LSB	RO

[a]RO = Read only

45.2.9.4.1 PD Assigned Power (13.3.11:0)

The PD Assigned Power is the maximum average available power at the PD PI.

45.2.9.5 PoDL PSE Status 4 register (Register 13.4)

The PoDL PSE Status 4 Register is defined if cable resistance measurement is supported.

Table 45–341b—PoDL PSE Status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.4.15:12	Reserved	Value always zero	RO
13.4.11:0	PD Requested Power	PD Requested Power, 0.025 W per LSB	RO

[a]RO = Read only

45.2.9.5.1 PD Requested Power (13.4.11:0)

The PD Requested Power is the requested average available power at the PD PI.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface[6]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.3 PMA/PMD management functions

Insert the following new rows after the MM151 row in the table in 45.5.3.3:

Item	Feature	Subclause	Value/Comment	Status	Support
MM152	Bits 1.2100.3:0 are ignored when Auto-Negotiation enable bit 7.512.12 is set to one	45.2.1.185.2		PMA:M	Yes [ ] N/A [ ]
MM153	A reset sets all 10BASE-T1L PMA registers to their default states	45.2.1.186a.1		PMA:M	Yes [ ] N/A [ ]
MM154	10BASE-T1L PMA returns a one in bit 1.2294.15 when a reset is in progress; otherwise, it returns a value of zero	45.2.1.186a.1		PMA:M	Yes [ ] N/A [ ]
MM155	The control and management interface is restored to operation within 0.5 s from the setting of bit 1.2294.15	45.2.1.186a.1		PMA:M	Yes [ ] N/A [ ]
MM156	During a reset, the 10BASE-T1L PMA responds to reads from register bits 1.2294.15, 1.8.15:14, and 1.0.15	45.2.1.186a.1		PMA:M	Yes [ ] N/A [ ]
MM157	Setting either 1.2294.15 or 1.0.15 sets the other	45.2.1.186a.1		PMA:M	Yes [ ] N/A [ ]
MM158	Clearing either 1.2294.15 or 1.0.15 clears the other	45.2.1.186a.1		PMA:M	Yes [ ] N/A [ ]
MM159	Setting either 1.2294.15 or 1.0.15 resets the 10BASE-T1L PMA	45.2.1.186a.1		PMA:M	Yes [ ] N/A [ ]
MM160	When bit 1.2294.14 is set to one, the 10BASE-T1L PMA disables output on the transmit path	45.2.1.186a.2		PMA:M	Yes [ ] N/A [ ]
MM161	When bit 1.2294.14 is set to zero, the 10BASE-T1L PMA enables output on the transmit path	45.2.1.186a.2		PMA:M	Yes [ ] N/A [ ]
MM162	Setting either 1.2294.14 or 1.9.0 sets the other	45.2.1.186a.2		PMA:M	Yes [ ] N/A [ ]
MM163	Clearing either 1.2294.14 or 1.9.0 clears the other	45.2.1.186a.2		PMA:M	Yes [ ] N/A [ ]
MM164	Setting either 1.2294.14 or 1.9.0 disables the transmitter	45.2.1.186a.2		PMA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM165	10BASE-T1L Transmit voltage amplitude control when Auto-Negotiation is not implemented or is not enabled	45.2.1.186a.3	1 = 10BASE-T1L PMA transmits using 2.4 Vpp operating mode 0 = 10BASE-T1L PMA transmits using 1.0 Vpp operating mode	PMA:M	Yes [ ] N/A [ ]
MM166	When Auto-Negotiation is implemented and enabled, setting bit 1.2294.12 has no effect	45.2.1.186a.3		PMA:M	Yes [ ] N/A [ ]
MM167	While in low-power mode, the device responds to management transactions necessary to exit the low-power mode	45.2.1.186a.4		PMA:M	Yes [ ] N/A [ ]
MM168	Setting either 1.2294.11 or 1.0.11 sets the other	45.2.1.186a.4		PMA:M	Yes [ ] N/A [ ]
MM169	Clearing either 1.2294.11 or 1.0.11 clears the other	45.2.1.186a.4		PMA:M	Yes [ ] N/A [ ]
MM170	Setting either 1.2294.11 or 1.0.11 puts the 10BASE-T1L PMA in low-power mode	45.2.1.186a.4		PMA:M	Yes [ ] N/A [ ]
MM171	10BASE-T1L EEE functionality when Auto-Negotiation is not implemented or is not enabled	45.2.1.186a.5	1 = PHY operates with EEE enabled 0 = PHY operates with EEE disabled	PMA:M	Yes [ ] N/A [ ]
MM172	When Auto-Negotiation is implemented and enabled, setting bit 1.2294.10 has no effect	45.2.1.186a.5		PMA:M	Yes [ ] N/A [ ]
MM173	When bit 1.2294.0 is set to one, the 10BASE-T1L PMA is placed into near-end loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.1.186a.6		PMA:M	Yes [ ] N/A [ ]
MM174	Setting either 1.2294.0 or 1.0.0 sets the other	45.2.1.186a.6		PMA:M	Yes [ ] N/A [ ]
MM175	Clearing either 1.2294.0 or 1.0.0 clears the other	45.2.1.186a.6		PMA:M	Yes [ ] N/A [ ]
MM176	Setting either 1.2294.0 or 1.0.0 enables loopback	45.2.1.186a.6		PMA:M	Yes [ ] N/A [ ]
MM177	The 10BASE-T1L PMA that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2295.1	45.2.1.186b.7		PMA:M	Yes [ ] N/A [ ]
MM178	The 10BASE-T1L PMA receive fault bit is implemented with latching high behavior	45.2.1.186b.7		PMA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM179	The 10BASE-T1L PMA receive link status bit is implemented with latching low behavior	45.2.1.186b.8		PMA:M	Yes [ ] N/A [ ]
MM180	A reset sets all 10BASE-T1S PMA registers to their default states	45.2.1.186d.1		PMA:M	Yes [ ] N/A [ ]
MM181	10BASE-T1S PMA returns a one in bit 1.2297.15 when a reset is in progress; otherwise, it returns a value of zero	45.2.1.186d.1		PMA:M	Yes [ ] N/A [ ]
MM182	The control and management interface is restored to operation within 0.5 s from the setting of bit 1.2297.15	45.2.1.186d.1		PMA:M	Yes [ ] N/A [ ]
MM183	During a reset, the 10BASE-T1S PMA responds to reads from register bits 1.2297.15, 1.8.15:14, and 1.0.15	45.2.1.186d.1		PMA:M	Yes [ ] N/A [ ]
MM184	Setting either 1.2297.15 or 1.0.15 sets the other	45.2.1.186d.1		PMA:M	Yes [ ] N/A [ ]
MM185	Clearing either 1.2297.15 or 1.0.15 clears the other	45.2.1.186d.1		PMA:M	Yes [ ] N/A [ ]
MM186	Setting either 1.2297.15 or 1.0.15 resets the 10BASE-T1S PMA	45.2.1.186d.1		PMA:M	Yes [ ] N/A [ ]
MM187	When bit 1.2297.14 is set to one, the 10BASE-T1S PMA disables output on the transmit path	45.2.1.186d.2		PMA:M	Yes [ ] N/A [ ]
MM188	When bit 1.2297.14 is set to zero, the 10BASE-T1S PMA enables output on the transmit path	45.2.1.186d.2		PMA:M	Yes [ ] N/A [ ]
MM189	Setting either 1.2297.14 or 1.0.14 sets the other	45.2.1.186d.2		PMA:M	Yes [ ] N/A [ ]
MM190	Clearing either 1.2297.14 or 1.0.14 clears the other	45.2.1.186d.2		PMA:M	Yes [ ] N/A [ ]
MM191	Setting either 1.2297.14 or 1.0.14 disables the transmitter	45.2.1.186d.2		PMA:M	Yes [ ] N/A [ ]
MM192	While in low-power mode, the device responds to management transactions necessary to exit the low-power mode	45.2.1.186d.3		PMA:M	Yes [ ] N/A [ ]
MM193	Setting either 1.2297.11 or 1.0.11 sets the other	45.2.1.186d.3		PMA:M	Yes [ ] N/A [ ]
MM194	Clearing either 1.2297.11 or 1.0.11 clears the other	45.2.1.186d.3		PMA:M	Yes [ ] N/A [ ]
MM195	Setting either 1.2297.11 or 1.0.11 puts the 10BASE-T1S PMA in low-power mode	45.2.1.186d.3		PMA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM196	When bit 1.2297.10 is set to one, the 10BASE-T1S PMA is configured to operate in multidrop mode	45.2.1.186d.4		PMA:M	Yes [ ] N/A [ ]
MM197	If multidrop mode is not supported according to bit 1.2298.10, writing to bit 1.2297.10 has no effect, and the PCS operates in half duplex mode with bits 3.2291.8 and 0.8 set to one	45.2.1.186d.4		PMA:M	Yes [ ] N/A [ ]
MM198	When bit 1.2297.0 is set to one, the 10BASE-T1S PMA is placed into loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.1.186d.5		PMA:M	Yes [ ] N/A [ ]
MM199	Setting either 1.2297.0 or 1.0.0 sets the other	45.2.1.186d.5		PMA:M	Yes [ ] N/A [ ]
MM200	Clearing either 1.2297.0 or 1.0.0 clears the other	45.2.1.186d.5		PMA:M	Yes [ ] N/A [ ]
MM201	Setting either 1.2297.0 or 1.0.0 enables loopback	45.2.1.186d.5		PMA:M	Yes [ ] N/A [ ]
MM202	The 10BASE-T1S PMA that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2298.1	45.2.1.186e.5		PMA:M	Yes [ ] N/A [ ]
MM203	The 10BASE-T1S PMA receive fault bit is implemented with latching high behavior	45.2.1.186e.5		PMA:M	Yes [ ] N/A [ ]

45.5.3.7 PCS management functions

Insert the following new rows after the RM157 row in the table in 45.5.3.7:

Item	Feature	Subclause	Value/Comment	Status	Support
RM158	This action sets all 10BASE-T1L PCS registers to their default states	45.2.3.68a.1		PCS:M	Yes [ ] N/A [ ]
RM159	The 10BASE-T1L PCS returns a value of one in bit 3.2278.15 when a reset is in progress; otherwise, returns a value of zero	45.2.3.68a.1		PCS:M	Yes [ ] N/A [ ]
RM160	The control and management interface is restored to operation within 0.5 s from the setting of bit 3.2278.15	45.2.3.68a.1		PCS:M	Yes [ ] N/A [ ]
RM161	During a reset, the 10BASE-T1L PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2278.15; reads for all other bits are ignored	45.2.3.68a.1		PCS:M	Yes [ ] N/A [ ]
RM162	Setting either 3.2278.15 or 3.0.15 sets the other	45.2.3.68a.1		PCS:M	Yes [ ] N/A [ ]
RM163	Clearing either 3.2278.15 or 3.0.15 clears the other	45.2.3.68a.1		PCS:M	Yes [ ] N/A [ ]
RM164	Setting either 3.2278.15 or 3.0.15 resets the 10BASE-T1L PCS	45.2.3.68a.1		PCS:M	Yes [ ] N/A [ ]
RM165	When bit 3.2278.14 is set to one, the 10BASE-T1L PCS is set to loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.3.68a.2		PCS:M	Yes [ ] N/A [ ]
RM166	Setting either 3.2278.14 or 3.0.14 sets the other	45.2.3.68a.2		PCS:M	Yes [ ] N/A [ ]
RM167	Clearing either 3.2278.14 or 3.0.14 clears the other	45.2.3.68a.2		PCS:M	Yes [ ] N/A [ ]
RM168	Setting either 3.2278.14 or 3.0.14 enables loopback	45.2.3.68a.2		PCS:M	Yes [ ] N/A [ ]
RM169	A write to the 10BASE-T1L PCS status 1 register has no effect	45.2.3.68b		PCS:M	Yes [ ] N/A [ ]
RM170	Bit 3.2279.11 is implemented with latching high behavior	45.2.3.68b.1		PCS:M	Yes [ ] N/A [ ]
RM171	Bit 3.2279.10 is implemented with latching high behavior	45.2.3.68b.2		PCS:M	Yes [ ] N/A [ ]
RM172	Bit 3.2279.7 is implemented with latching high behavior	45.2.3.68b.5		PCS:M	Yes [ ] N/A [ ]
RM173	Bit 3.2279.2 is implemented with latching low behavior	45.2.3.68b.6		PCS:M	Yes [ ] N/A [ ]
RM174	This action sets all 10BASE-T1S PCS registers to their default states	45.2.3.68c.1		PCS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM175	The 10BASE-T1S PCS returns a value of one in bit 3.2291.15 when a reset is in progress; otherwise, returns a value of zero	45.2.3.68c.1		PCS:M	Yes [ ] N/A [ ]
RM176	The control and management interface is restored to operation within 0.5 s from the setting of bit 3.2291.15	45.2.3.68c.1		PCS:M	Yes [ ] N/A [ ]
RM177	During a reset, the 10BASE-T1S PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2291.15; reads for all other bits are ignored	45.2.3.68c.1		PCS:M	Yes [ ] N/A [ ]
RM178	Setting either 3.2291.15 or 3.0.15 sets the other	45.2.3.68c.1		PCS:M	Yes [ ] N/A [ ]
RM179	Clearing either 3.2291.15 or 3.0.15 clears the other	45.2.3.68c.1		PCS:M	Yes [ ] N/A [ ]
RM180	Setting either 3.2291.15 or 3.0.15 resets the 10BASE-T1S PCS	45.2.3.68c.1		PCS:M	Yes [ ] N/A [ ]
RM181	When bit 3.2291.14 is set to one, the 10BASE-T1S PCS is set to loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.3.68c.2		PCS:M	Yes [ ] N/A [ ]
RM182	Setting either 3.2291.14 or 3.0.14 sets the other	45.2.3.68c.2		PCS:M	Yes [ ] N/A [ ]
RM183	Clearing either 3.2291.14 or 3.0.14 clears the other	45.2.3.68c.2		PCS:M	Yes [ ] N/A [ ]
RM184	Setting either 3.2291.14 or 3.0.14 enables loopback	45.2.3.68c.2		PCS:M	Yes [ ] N/A [ ]
RM185	Bit 3.2291.8 or 0.8 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one	45.2.3.68c.3		PCS:M	Yes [ ] N/A [ ]
RM186	Setting either 3.2291.8 or 0.8 sets the other	45.2.3.68c.3		PCS:M	Yes [ ] N/A [ ]
RM187	Clearing either 3.2291.8 or 0.8 clears the other	45.2.3.68c.3		PCS:M	Yes [ ] N/A [ ]
RM188	The 10BASE-T1S PCS fault bit is implemented with latching high behavior	45.2.3.68d.1		PCS:M	Yes [ ] N/A [ ]
RM189	A write to the 10BASE-T1S PCS status register has no effect	45.2.3.68d		PCS:M	Yes [ ] N/A [ ]
RM190	A write to the 10BASE-T1S PCS diagnostic register has no effect	45.2.3.68e		PCS:M	Yes [ ] N/A [ ]
RM191	Remote jabber count does not wrap	45.2.3.68e.1		PCS:M	Yes [ ] N/A [ ]
RM192	Writes to PCS diagnostic 2 register have no effect	45.2.3.68f		PCS:M	Yes [ ] N/A [ ]

45.5.3.9 Auto-Negotiation management functions

Insert the following new rows after the AM93 row in the table in 45.5.3.9:

Item	Feature	Subclause	Value/Comment	Status	Support
AM94	When bit 7.526.15 is set to one, the PHY advertises 10BASE-T1L capability	45.2.7.25.1		AN:M	Yes [ ] N/A [ ]
AM95	When bit 7.526.15 is set to zero, the PHY does not advertise 10BASE-T1L capability	45.2.7.25.1		AN:M	Yes [ ] N/A [ ]
AM96	If a 10BASE-T1L PHY supports EEE ability and desires to operate in EEE mode, bit 7.526.14 is set to one	45.2.7.25.2		AN:M	Yes [ ] N/A [ ]
AM97	If a 10BASE-T1L PHY supports the 2.4 Vpp operating mode, bit 7.526.13 is set to one	45.2.7.25.3		AN:M	Yes [ ] N/A [ ]
AM98	When bit 7.526.12 is set to one, a request to operate the 10BASE-T1L PHY in increased transmit level mode is advertised	45.2.7.25.4		AN:M	Yes [ ] N/A [ ]
AM99	When bit 7.526.12 is set to zero, a request to operate the 10BASE-T1L PHY in increased transmit level mode is not advertised	45.2.7.25.4		AN:M	Yes [ ] N/A [ ]
AM100	When bit 7.526.7 is set to one, the PHY advertises 10BASE-T1S full duplex ability	45.2.7.25.5		AN:M	Yes [ ] N/A [ ]
AM101	When bit 7.526.7 is set to zero, the PHY does not advertise 10BASE-T1S full duplex ability	45.2.7.25.5		AN:M	Yes [ ] N/A [ ]
AM102	When bit 7.526.6 is set to one, the PHY advertises 10BASE-T1S halfduplex capability	45.2.7.25.6		AN:M	Yes [ ] N/A [ ]
AM103	When bit 7.526.6 is set to zero, the PHY does not advertise 10BASE-T1S half duplex capability	45.2.7.25.6		AN:M	Yes [ ] N/A [ ]
AM104	Writing to the 10BASE-T1 AN status register has no effect	45.2.7.26		AN:M	Yes [ ] N/A [ ]
AM105	When the AN process is complete, the 10BASE-T1 AN status register reflects the contents of the link partner’s 10BASE-T1 AN control register	45.2.7.26		AN:M	Yes [ ] N/A [ ]

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.4 PHY types optionally supporting EEE

Insert the following new row after the 10BASE-Te row in Table 78–1:

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
10BASE-T1L	146

78.2 LPI mode timing parameters description

Insert the following new row at the beginning of Table 78–2:

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

PHY or interface type	T_s (µs)		T_q (µs)		T_r (µs)	
	Min	Max	Min	Max	Min	Max
10BASE-T1L	20	20	6 000	6 000	250	250

78.5 Communication link access latency

Insert the following new row at the beginning of Table 78–4:

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (µs)	T_{w_phy} (min) (µs)	$T_{phy\_shrink\_tx}$ (max) (µs)	$T_{phy\_shrink\_rx}$ (max) (µs)	$T_{w\_sys\_rx}$ (min) (µs)
10BASE-T1L		270	250.5	10	240	20

98. Auto-Negotiation for single differential-pair media

98.2 Functional specifications

98.2.1 Transmit function requirements

Insert the following new paragraph at the end of the introductory text of 98.2.1:

Two different Auto-Negotiation speeds are defined in this subclause. A PHY shall support at least one of these Auto-Negotiation speeds. The two speeds are referred to as *high-speed mode*, or HSM, and *low-speed mode*, or LSM. If Auto-Negotiation is implemented, 1000BASE-T1, 100BASE-T1, and 10BASE-T1S PHYs shall support HSM and may optionally support LSM. For link segments with high insertion loss and those requiring 10BASE-T1L, LSM is provided to enable the full reach capability. If Auto-Negotiation is implemented, 10BASE-T1L PHYs shall support LSM and may optionally support HSM. When performing Auto-Negotiation in high-speed mode, DME pages are transmitted at a nominal rate of 16.667 Mb/s. In low-speed mode, DME pages are transmitted at a nominal rate of 625 kb/s. Subclause 98.5.6 describes the behavior to automatically choose between the different Auto-Negotiation speeds when a PHY supports both.

98.2.1.1 DME transmission

98.2.1.1.1 DME page encoding

Change the second paragraph in 98.2.1.1.1 as follows:

The first 26 transition positions contain the Start Delimiter, which marks the beginning of the page. The Start Delimiter contains a transition from quiet to active at position 1. For HSM Auto-Negotiation, this transition is followed by transitions at positions 2, 3, 5, 7, 8, 12, 13, 14, 15, 19, 21, 24, 25, 26 and no transitions at the remaining positions. For LSM Auto-Negotiation, this transition is followed by transitions at positions 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 15, 16, 18, 19, 20, 22, 23, 24, 26 and no transitions at the remaining positions.

98.2.1.1.2 DME page timing

Change the first paragraph in 98.2.1.1.2 as follows:

The timing parameters for DME pages shall be followed as in Table 98–1. The transition positions within a DME page are spaced with a period of T1. T2 is the separation between clock transitions. T3 is the time from a clock transition to a data transition representing a one. ~~The period, T1, shall be 30.0 ns ± 0.01%. Transitions shall occur within ± 0.8 ns of their ideal positions.~~ When operating in high-speed mode, transitions shall occur within ± 0.8 ns of their ideal positions. When operating in low-speed mode, transitions shall occur within ± 10 ns of their ideal positions.

Change Table 98-1 as follows:

Table 98–1—DME page timing summary

	Parameters	Mode	Min	Typ	Max	Units
T1	Transmit position spacing (period)	high-speed	29.997	30	30.003	ns
		low-speed	799.96	800	800.04	
T2	Clock transition to clock transition	high-speed	59.8	60	60.2	ns
		low-speed	1590	1600	1610	
T3	Clock transition to data transition (data = 1)	high-speed	29.9	30	30.1	ns
		low-speed	795	800	805	
T4a	+1 to –1 or –1 to +1 transitions in a DME page	high-speed	79	—	143	—
		low-speed	84	—	148	
T4b	0 to ±1 or ±1 to 0 transitions in a DME page	high-speed	2	2	2	—
		low-speed	2	2	2	
T5	DME page width	high-speed	4679	4680	4681	ns
		low-speed	124 793	124 800	124 807	

98.2.1.1.3 DME page Delimiters

Change the first paragraph in 98.2.1.1.3 as follows:

The page is preceded by a unique Start Delimiter consisting of a 26 × T1 sequence that includes multiple DME transition violations. For a Start Delimiter starting with a 0 to +1 transition, the bit sequence for high-speed Auto-Negotiation mode is

+1 –1 +1 +1 –1 –1 +1 –1 –1 –1 –1 +1 –1 +1 –1 –1 –1 –1 +1 +1 –1 –1 –1 +1 –1 +1.

Insert the following new paragraph after the first paragraph in 98.2.1.1.3:

For a Start Delimiter starting with a 0 to +1 transition, the bit sequence for low-speed Auto-Negotiation mode is

+1 –1 +1 –1 +1 –1 +1 –1 +1 +1 –1 –1 +1 +1 –1 +1 +1 –1 +1 –1 –1 +1 –1 +1 +1 –1.

98.5 Detailed functions and state diagrams

98.5.1 State diagram variables

Insert the following new variable after the variable an_receive_idle:

ANSP

This variable contains the type of the selected Auto-Negotiation speed.
Values:
HSM: high-speed mode
LSM: low-speed mode

Insert the following new variable after the variable mr_restart_negotiation:

multispeed_autoneg_reset

See 98.5.6.1.

Change the variable power_on as follows:

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low-power mode set via 1000BASE-T1 PMA control register bit 1.2304.11 or via 10BASE-T1L PMA control register bit 1.2294.11.
Values:
false: the device is completely powered (default)
true: the device has not been completely powered

98.5.2 State diagram timers

Change 98.5.2 as follows:

All timers operate in the manner described in 40.4.5.2.

When operating in high-speed mode, the following timer value definitions shall apply:

backoff_timer_[HSM]

Timer for the random amount of time to wait for a page to arrive from the link partner before transmitting a page. The timer shall expire according to the formula below after being started.
If T[4] bit is 1, ~~then~~ the timer duration is ~~set as~~ (6805 ns to 6925 ns) + (random integer from 0 to 15) × (2120 ns to 2240 ns).
If T[4] bit is 0, ~~then~~ the timer duration is ~~set as~~ (7895 ns to 8015 ns) + (random integer from 0 to 15) × (2120 ns to 2240 ns).
A new random integer from 0 to 15 inclusive is generated every time the backoff_timer_[HSM] is started. The random value should be uniformly distributed.

blind_timer_[HSM]

Timer for the amount of time to blind the receiver after end of transmission to prevent the device from seeing its own echo. The timer shall expire 2000 ns to 2120 ns after being started.

break_link_timer_[HSM]

Timer for the amount of time to wait in ~~order~~TRANSMIT DISABLE to assure that the link partner will exit from either ACKNOWLEDGE DETECT or NEXT PAGE WAIT; effect on the link partner in other states is not defined~~enters a Link Fail state~~. The timer shall expire 300 µs to 305 µs after being started.

clock_detect_max_timer_[HSM]
Timer for the maximum time between detection of differential Manchester clock transitions. The clock_detect_max_timer_[HSM] shall expire 63 ns to 75 ns after being started or restarted.

clock_detect_min_timer_[HSM]
Timer for the minimum time between detection of differential Manchester clock transitions. The clock_detect_min_timer_[HSM] shall expire 45 ns to 57 ns after being started or restarted.

data_detect_max_timer_[HSM]
Timer for the maximum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_min_timer_[HSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_max_timer_[HSM] shall expire 33 ns to 45 ns from the last clock transition.

data_detect_min_timer_[HSM]
Timer for the minimum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_max_timer_[HSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_min_timer_[HSM] shall expire 15 ns to 27 ns from the last clock transition.

interval_timer_[HSM]
Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer_[HSM] shall expire 30 ns ± 0.01% from each clock pulse and data bit.

~~link_fail_inhibit_timer~~
~~Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 97 ms to 98 ms after entering the AN GOOD CHECK state.~~

~~NOTE—The link_fail_inhibit_timer expiration value is greater than the time required for the link partner to complete Auto-Negotiation after the local device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state.~~

page_test_max_timer_[HSM]
Timer for the maximum time between detection of start and end delimiters. The page_test_max_timer_[HSM] shall expire 4800 ns to 4920 ns after being started or restarted.

receive_DME_timer_[HSM]
Timer for the maximum amount of time to receive a complete page before timeout. The timer shall expire 6805 ns to 6925 ns after being started.

rx_wait_timer_[HSM]
Timer for the maximum time between detection of DME pages. This timer is used to detect whether the link partner is transmitting DME pages. The rx_wait_timer_[HSM] shall expire 15 µs to 17 µs after being started or restarted.

silent_timer_[HSM]
Timer for the amount of time to wait after receiving a page before transmitting a page. The timer shall expire 2120 ns to 2240 ns after being started.

When operating in low-speed mode, the following timer value definitions shall apply:

backoff_timer_[LSM]
Timer for the random amount of time to wait for a page to arrive from the link partner before transmitting a page. The timer shall expire according to the formula below after being started. If T[4] bit is 1, the timer duration is (156 300 ns to 159 500 ns) + (random integer from 0 to 15) × (31 400 ns to 34 600 ns).

If T[4] bit is 0, the timer duration is (172 800 ns to 176 000 ns) + (random integer from 0 to 15) × (31 400 ns to 34 600 ns).
A new random integer from 0 to 15 inclusive is generated every time the backoff_timer_[LSM] is started. The random value should be uniformly distributed.

blind_timer_[LSM]
: Timer for the amount of time to blind the receiver after end of transmission to prevent the device from seeing its own echo. The timer shall expire 28 200 ns to 31 400 ns after being started.

break_link_timer_[LSM]
: Timer for the amount of time to wait in TRANSMIT DISABLE to assure that the link partner will exit from either ACKNOWLEDGE DETECT or NEXT PAGE WAIT; effect on the link partner in other states is not defined. The timer shall expire 8000 µs to 8133 µs after being started.

clock_detect_max_timer_[LSM]
: Timer for the maximum time between detection of differential Manchester clock transitions. The clock_detect_max_timer_[LSM] shall expire 1680 ns to 2000 ns after being started or restarted.

clock_detect_min_timer_[LSM]
: Timer for the minimum time between detection of differential Manchester clock transitions. The clock_detect_min_timer_[LSM] shall expire 1200 ns to 1520 ns after being started or restarted.

data_detect_max_timer_[LSM]
: Timer for the maximum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_min_timer_[LSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_max_timer_[LSM] shall expire 880 ns to 1200 ns from the last clock transition.

data_detect_min_timer_[LSM]
: Timer for the minimum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_max_timer_[LSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_min_timer_[LSM] shall expire 400 ns to 720 ns from the last clock transition.

interval_timer_[LSM]
: Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer_[LSM] shall expire 800 ns ± 0.005% from each clock pulse and data bit.

page_test_max_timer_[LSM]
: Timer for the maximum time between detection of start and end delimiters. The page_test_max_timer_[LSM] shall expire 128 000 ns to 131 200 ns after being started or restarted.

receive_DME_timer_[LSM]
: Timer for the maximum amount of time to receive a complete page before timeout. The timer shall expire 156 300 ns to 159 500 ns after being started.

rx_wait_timer_[LSM]
: Timer for the maximum time between detection of DME pages. This timer is used to detect whether the link partner is transmitting DME pages. The rx_wait_timer_[LSM] shall expire 330 µs to 370 µs after being started or restarted.

silent_timer_[LSM]
: Timer for the amount of time to wait after receiving a page before transmitting a page. The timer shall expire 31 400 ns to 34 600 ns after being started.

Depending on the selected PHY type, done by Auto-Negotiation, the following timer values shall be used:

link_fail_inhibit_timer_[HCD]
: Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will be considered "failed" only if the link_fail_inhibit_timer_[HCD] has expired and the link has still not gone into the link_status=OK state. The expiration time of the link_fail_inhibit_timer_[HCD] shall be dependent on the selected PHY type. For all PHY types, except 10BASE-T1L and 10BASE-T1S, this timer shall expire 97 ms to 98 ms after entering the AN GOOD CHECK state. For a 10BASE-T1L PHY, this timer shall expire 3030 ms to 3090 ms after entering the AN GOOD CHECK state. For a 10BASE-T1S PHY, this timer shall expire 400 ms to 405 ms after entering the AN GOOD CHECK state.

NOTE—The link_fail_inhibit_timer_[HCD] expiration value is greater than the time required for the link partner to complete Auto-Negotiation after the local device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state.

98.5.5 State diagrams

Replace Figure 98-7 with the following figure:

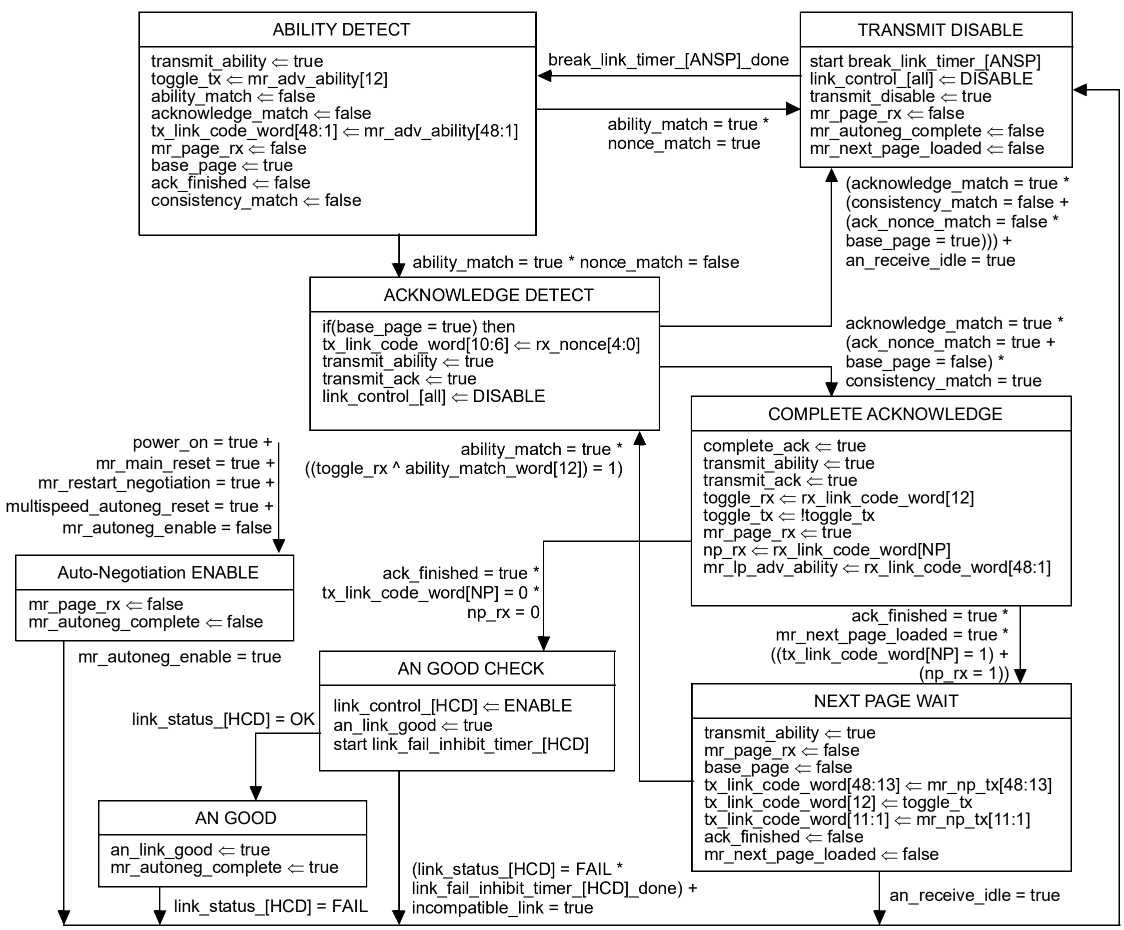


Figure 98–7—Arbitration state diagram

Replace Figure 98-8 with the following figure:

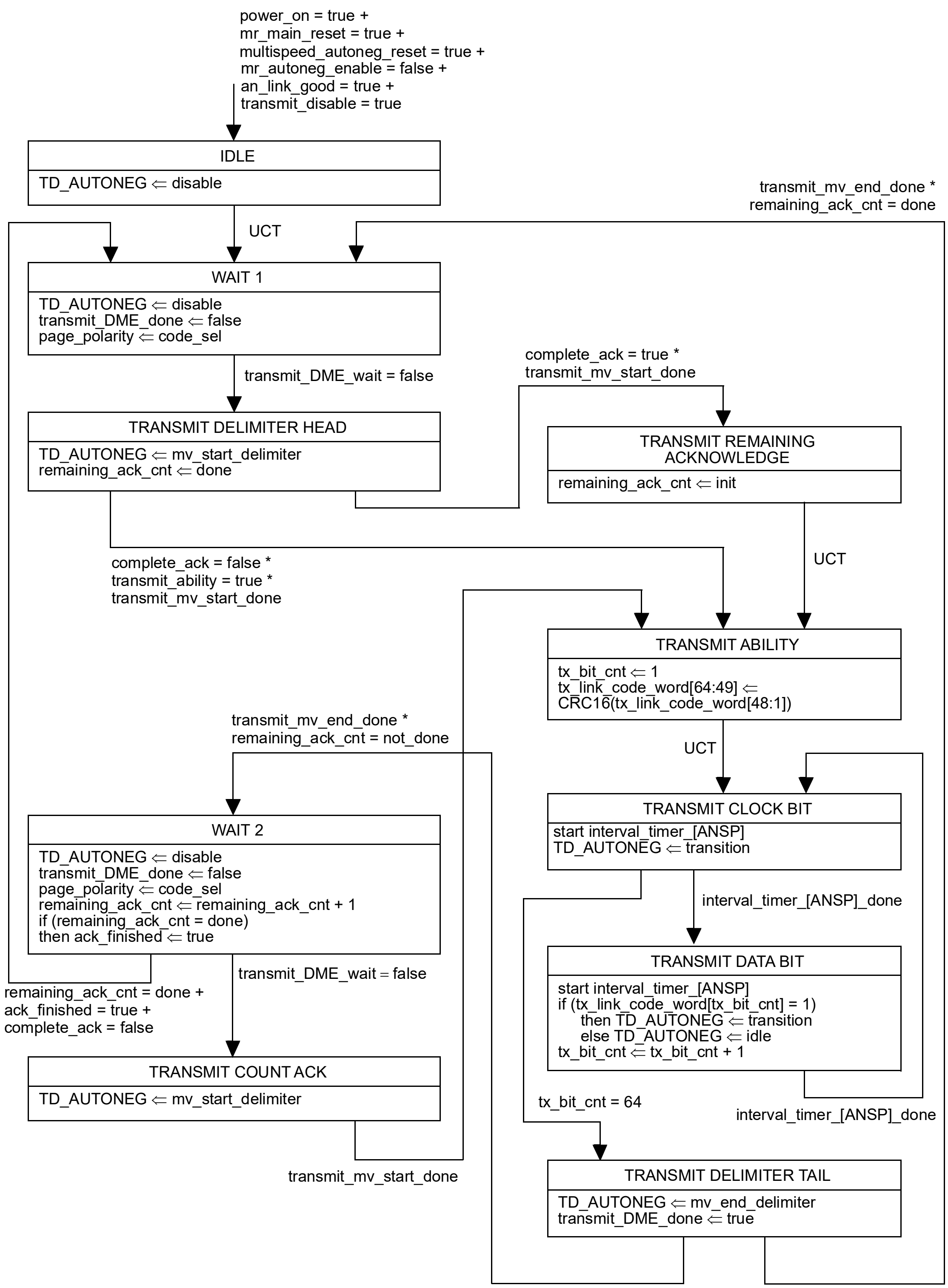


Figure 98–8—Transmit state diagram

Replace Figure 98-9 with the following figure:

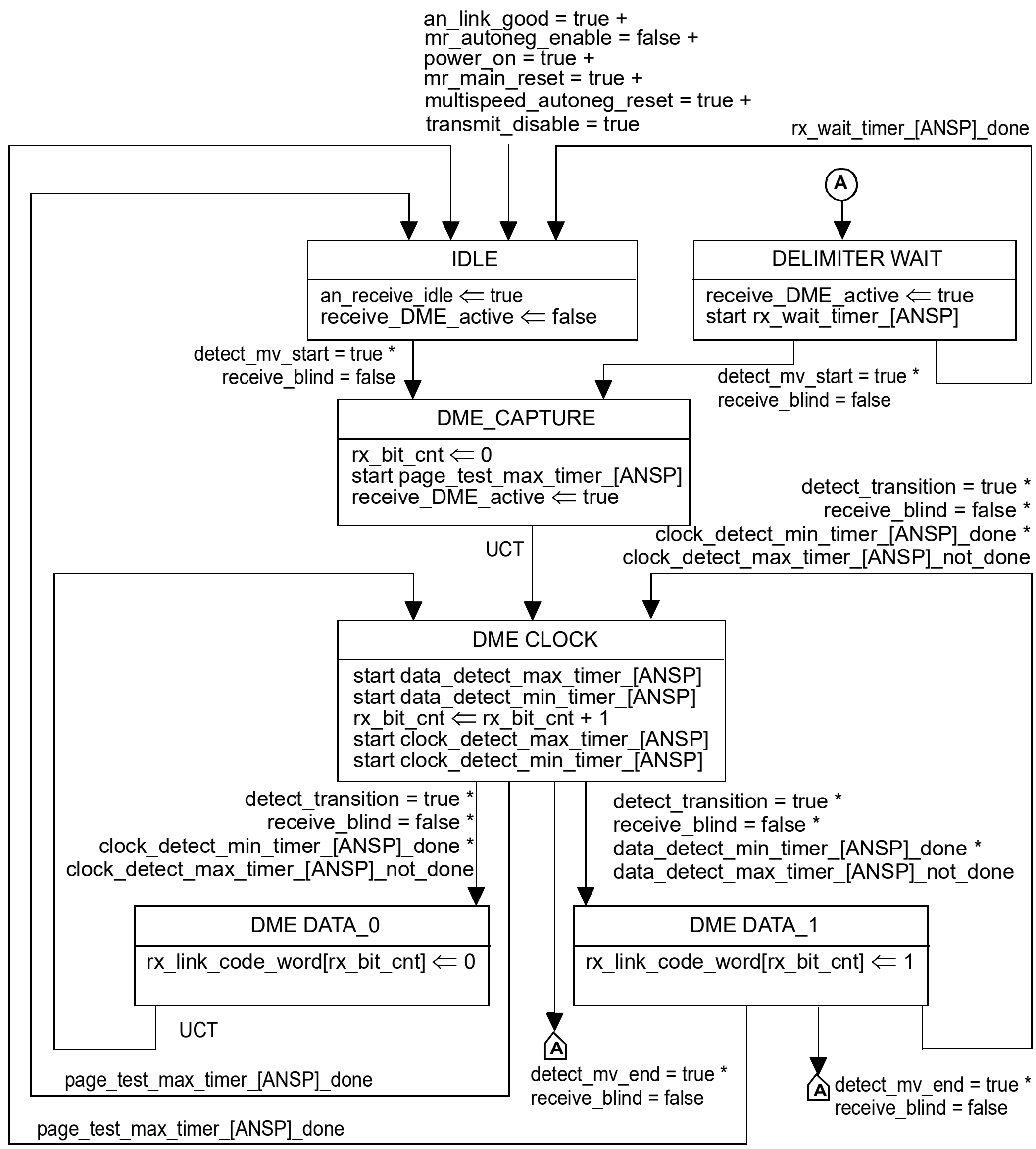


Figure 98–9—Receive state diagram

Replace Figure 98-10 with the following figure:

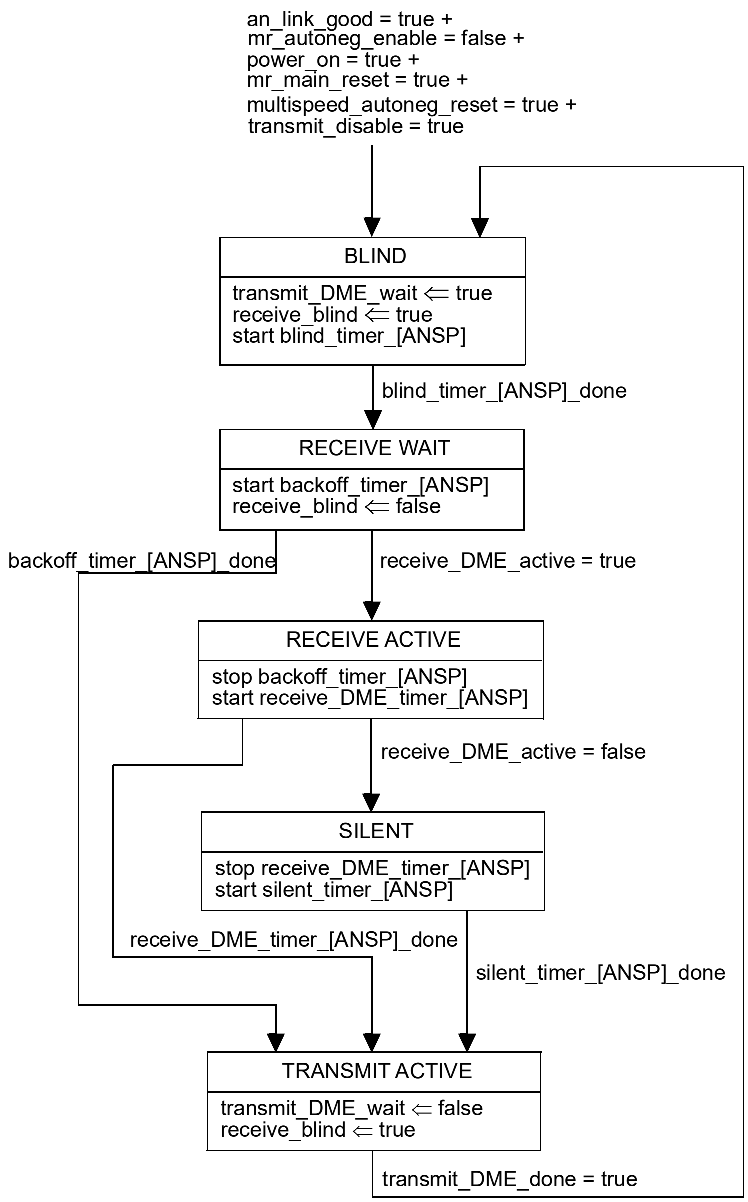


Figure 98–10—Half-duplex state diagram

Insert the following new subclauses (98.5.6 through 98.5.6.3, including Figure 98-11) after 98.5.5:

98.5.6 High-speed and low-speed Auto-Negotiation modes

A PHY supporting two different Auto-Negotiation speeds, as described in 98.2.1.1.2, shall implement the behavior shown in Figure 98–11. Figure 98–11 determines the mode used for the timers in Figure 98–7, Figure 98–8, Figure 98–9, Figure 98–10, and Figure 98–11 through the variable ANSP and synchronizes them through the variable multispeed_autoneg_reset.

A PHY supporting only one Auto-Negotiation speed shall implement the behavior as shown in Figure 98–7, Figure 98–8, Figure 98–9, and Figure 98–10, using the associated timer values for high-speed mode (HSM) or low-speed mode (LSM) Auto-Negotiation as described in 98.5.2.

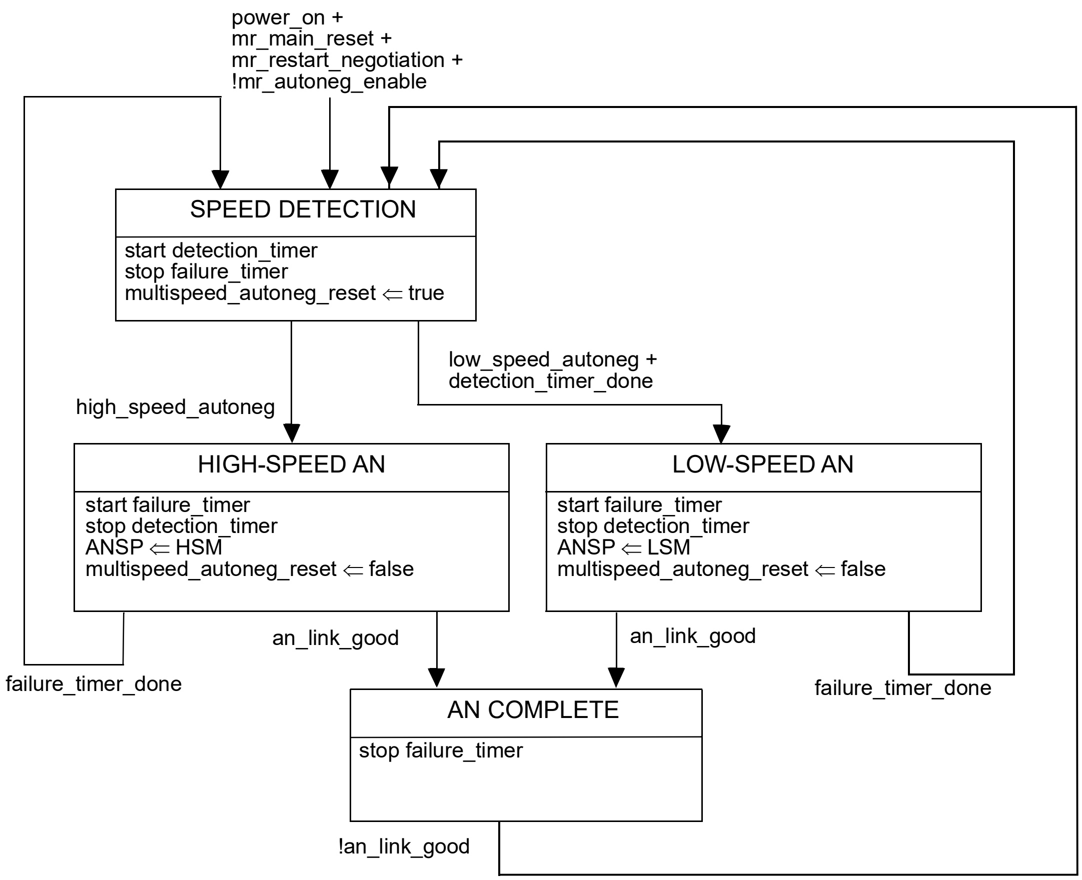


Figure 98–11—Auto-Negotiation—high-speed mode and low-speed mode selection

98.5.6.1 Variables

an_link_good
See 98.5.1.

ANSP
See 98.5.1.

mr_autoneg_enable
See 98.5.1.

mr_main_reset
: See 98.5.1.

mr_restart_negotiation
: See 98.5.1.

multispeed_autoneg_reset
: If two different Auto-Negotiation speeds are implemented and this variable is set to true by the state diagram in Figure 98–11, then the state diagrams in Figure 98–7, Figure 98–8, Figure 98–9, and Figure 98–10 are restarted. If only single speed Auto-Negotiation is implemented, then this variable remains set to false.
: Values: true: Auto-Negotiation state diagrams are restarted
: false: Auto-Negotiation state diagrams are in normal operation

power_on
: See 98.5.1.

98.5.6.2 Functions

high_speed_autoneg
: This function returns true if at least the last 12 received DME pulses are within the allowed range for the high-speed Auto-Negotiation communication (15 ns to 135 ns pulse width) including the violations of the DME encoding within the start delimiter; otherwise, this function returns false.
: Values: true or false

low_speed_autoneg
: This function returns false if at least the last 12 received DME pulses are within the allowed range for the low-speed Auto-Negotiation communication (400 ns to 2000 ns pulse width) including the violations of the DME encoding within the start delimiter; otherwise, this function returns false.
: Values: true or false

98.5.6.3 Timers

All timers operate in the manner described in 40.4.5.2.

detection_timer
: This timer limits the maximum time for detection of Auto-Negotiation frames sent by the far end PHY, before starting to send its own Auto-Negotiation frames at low-speed. This timer is not automatically restarted after expiration. A new random integer from 0 to 15 inclusive is generated every time the detection_timer is started. The random value should be uniformly distributed.
: Timer value: (10 ms ± 0.1 ms) + (random integer from 0 to 15) × (0.5 ms ± 0.05 ms)

failure_timer
: This timer limits the maximum time for the underlying Auto-Negotiation state diagrams to complete the Auto-Negotiation process before restarting the Auto-Negotiation process. This timer is not automatically restarted after expiration.
: Timer value: 250 ms ± 1 ms

98.6 Protocol implementation conformance statement (PICS) proforma for Clause 98, Auto-Negotiation for Single Differential-Pair Media[7]

Insert the following new subclause (98.6.2a) after 98.6.2.2:

98.6.2a Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*ANSM	Auto-Negotiation Speed Mode	98.5.6		O	Yes [ ] No [ ]
*HSM	High-Speed Mode	98.5.2, 98.5.6		O	Yes [ ] No [ ]
*LSM	Low-Speed Mode	98.5.2, 98.5.6		O	Yes [ ] No [ ]
*10T1L	10BASE-T1L PHY type	98.5.2		O	Yes [ ] No [ ]
*10T1S	10BASE-T1S PHY type	98.5.2		O	Yes [ ] No [ ]

98.6.3 General

Insert the following new rows at the end of the table in 98.6.3:

Item	Feature	Subclause	Value/Comment	Status	Support
G3	PHY support for High-Speed Mode	98.2.1, 98.5.6		ANSM: O.1	Yes [ ] No [ ] N/A [ ]
G4	PHY support for Low-Speed Mode	98.2.1, 98.5.2, 98.5.6		ANSM: O.1	Yes [ ] No [ ] N/A [ ]

98.6.4 DME transmission

Change the table in 98.6.4 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
DME8	The timing parameters for DME pages.~~DME page period, T1~~	98.2.1.1.2	~~30.0 ns ± 0.01%~~ See Table 98–1	M	Yes [ ]
DME9	DME page transitions in high-speed mode	98.2.1.1.2	Occur within ± 0.8 ns of their ideal position	HSM: M	Yes [ ] N/A [ ]
DME9a	DME page transitions in low-speed mode	98.2.1.1.2	Occur within ± 10 ns of their ideal position	LSM: M	Yes [ ] N/A [ ]
…					

[7]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

98.6.8 State diagram and variable definitions

Change the table in 98.6.8 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
SD3	backoff_timer_[HSM]	98.5.2	Expire according to the formula described in 98.5.2	HSM:M	Yes [ ] N/A [ ]
SD3a	backoff_timer_[LSM]	98.5.2	Expire according to the formula described in 98.5.2	LSM:M	Yes [ ] N/A [ ]
SD4	blind_timer_[HSM]	98.5.2	Expires 2000 ns to 2120 ns after being started	HSM:M	Yes [ ] N/A [ ]
SD4a	blind_timer_[LSM]	98.5.2	Expires 28 200 ns to 31 400 ns after being started	LSM:M	Yes [ ] N/A [ ]
SD5	break_link_timer_[HSM]	98.5.2	Expires 300 µs to 305 µs after being started	HSM:M	Yes [ ] N/A [ ]
SD5a	break_link_timer_[LSM]	98.5.2	Expires 8000 µs to 8133 µs after being started	LSM:M	Yes [ ] N/A [ ]
SD6	clock_detect_max_timer_[HSM]	98.5.2	Expires 63 ns to 75 ns after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD6a	clock_detect_max_timer_[LSM]	98.5.2	Expires 1680 ns to 2000 ns after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD7	clock_detect_min_timer_[HSM]	98.5.2	Expires 45 ns to 57 ns after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD7a	clock_detect_min_timer_[LSM]	98.5.2	Expires 1200 ns to 1520 ns after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD8	data_detect_max_timer_[HSM]	98.5.2	Expires 33 ns to 45 ns from the last clock transition	HSM:M	Yes [ ] N/A [ ]
SD8a	data_detect_max_timer_[LSM]	98.5.2	Expires 880 ns to 1200 ns from the last clock transition	LSM:M	Yes [ ] N/A [ ]
SD9	data_detect_min_timer_[HSM]	98.5.2	Expires 15 ns to 27 ns from the last clock transition	HSM:M	Yes [ ] N/A [ ]
SD9a	data_detect_min_timer_[LSM]	98.5.2	Expires 400 ns to 720 ns from the last clock transition	LSM:M	Yes [ ] N/A [ ]
SD10	interval_timer_[HSM]	98.5.2	Expires 30 ns ± 0.01% from each clock pulse and data bit	HSM:M	Yes [ ] N/A [ ]
SD10a	interval_timer_[LSM]	98.5.2	Expires 800 ns ± 0.005% from each clock pulse and data bit	LSM:M	Yes [ ] N/A [ ]
SD11	link_fail_inhibit_timer_[HCD]	98.5.2	Expires 97 ms to 98 ms after entering the AN LINK GOOD CHECK state	!10T1L: M	Yes [ ] N/A [ ]
SD11a	link_fail_inhibit_timer_[HCD] for 10BASE-T1L PHY	98.5.2	Expires 3030 ms to 3090 ms after entering the AN LINK GOOD CHECK state	10T1L: M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
SD11b	link_fail_inhibit_timer_[HCD] for 10BASE-T1S PHY	98.5.2	Expires 400 ms to 405 ms after entering the AN LINK GOOD CHECK state	10T1S:M	Yes [ ] N/A [ ]
SD12	page_test_max_timer_[HSM]	98.5.2	Expires 4800 ns to 4920 ns after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD12a	page_test_max_timer_[LSM]	98.5.2	Expires 128 000 ns to 131 200 ns after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD13	receive_DME_timer_[HSM]	98.5.2	Expires 6805 ns to 6925 ns after being started	HSM:M	Yes [ ] N/A [ ]
SD13a	receive_DME_timer_[LSM]	98.5.2	Expires 156 300 ns to 159 500 ns after being started	LSM:M	Yes [ ] N/A [ ]
SD14	rx_wait_timer_[HSM]	98.5.2	Expires 15 µs to 17 µs after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD14a	rx_wait_timer_[LSM]	98.5.2	Expires 330 µs to 370 µs after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD15	silent_timer_[HSM]	98.5.2	Expires 2120 ns to 2240 ns after being started	HSM:M	Yes [ ] N/A [ ]
SD15a	silent_timer_[LSM]	98.5.2	Expires 31 400 ns to 34 600 ns after being started	LSM:M	Yes [ ] N/A [ ]

Insert the following new subclause (98.6.9) after 98.6.8:

98.6.9 High-speed and low-speed Auto-Negotiation modes

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Supports two Auto-Negotiation speeds	98.5.6	Implements the state diagram in Figure 98–11	ANSM:M	Yes [ ] N/A [ ]
SM2	Supports only high-speed mode	98.5.6	Implements Figure 98–7, Figure 98–8, Figure 98–9, and Figure 98–10 using the timer values for high-speed mode	!LSM:M	Yes [ ] N/A [ ]
SM3	Supports only low-speed mode	98.5.6	Implements Figure 98–7, Figure 98–8, Figure 98–9, and Figure 98–10 using the timer values for low-speed mode	!HSM:M	Yes [ ] N/A [ ]

Change the title of Clause 104 as follows:

104. Power over Data Lines (PoDL) of Single~~ Balanced Twisted~~-Pair Ethernet

104.1 Overview

104.1.3 PoDL system types

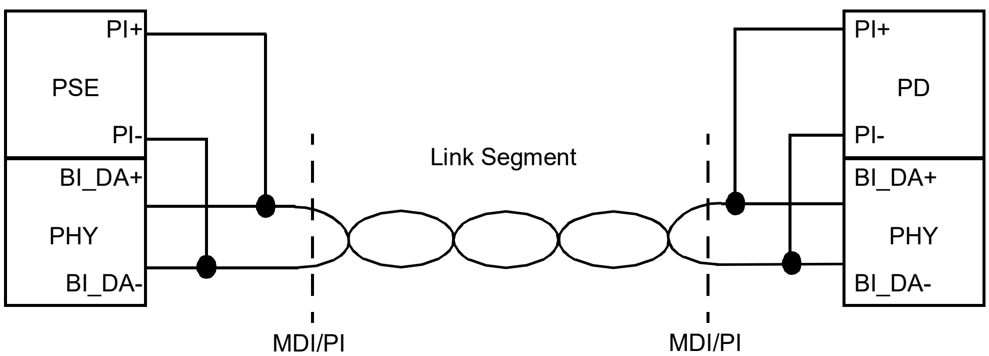
Change the text of 104.1.3 as follows:

A PoDL system consists of a PSE, a link segment, and a PD. PoDL systems are not specified for mixing segments.

A Type A or Type C PSE and Type A or Type C PD are~~is~~ compatible with 10BASE-T1S and 100BASE-T1 PHYs. A Type B or Type C PSE and Type B or Type C PD are~~is~~ compatible with 1000BASE-T1 PHYs. A Type C PSE and Type C PD are~~is~~ compatible with ~~both~~10BASE-T1S, 100BASE-T1, and 1000BASE-T1 PHYs. Type D PSEs and Type D PDs may be incompatible with IEEE 802.3 PHYs and may lack a data entity. A Type E PSE and Type E PD are compatible with 10BASE-T1L PHYs.

Figure 104–3 illustrates the block diagram for a PoDL system.

Replace Figure 104-3 with the following figure (in which MDI+ has been replaced with BI_DA+ and MDI- with BI_DA-):



NOTE—PI elements that prevent loading of the data signal by the PSE and PD are not shown. PHY elements that block dc are not shown.

Figure 104–3—PoDL system block diagram

104.2 Link segment

Change 104.2 as follows:

The dc loop resistance of the link segment shall be less than 6 Ω for ~~12 V unregulated classes~~classes 0 and 1. The dc loop resistance shall be less than 6.5 Ω for ~~12 V regulated, 24 V regulated and unregulated, and 48 V regulated classes~~classes 2 through 9. The link segment dc loop resistance shall be less than 65 Ω for classes 10 and 13. The link segment dc loop resistance shall be less than 25 Ω for classes 11 and 14. The link segment dc loop resistance shall be less than 9.5 Ω for classes 12 and 15.

104.3 Class power requirements

Change the text of 104.3 as follows:

PSEs and PDs are further categorized by their class. These classes and the relevant electrical specifications are shown in Table 104–1 and Table 104–1a.

Change title of Table 104-1 as shown:

Table 104–1—Class power requirements matrix for PSE, PI, and PD for classes 0 through 9

Insert the following new table (Table 104-1a) after Table 104-1:

Table 104–1a—Class power requirements matrix for PSE, PI, and PD for classes 10 through 15

Class	10	11	12	13	14	15
$V_{PSE(max)}$ (V)	30	30	30	58	58	58
$V_{PSE\_OC(min)}$ (V)	20	20	20	50	50	50
$V_{PSE(min)}$ (V)	20	20	20	50	50	50
$I_{PI(max)}$ (mA)	92	240	632	231	600	1579
$P_{class(min)}$ (W)	1.85	4.8	12.63	11.54	30	79
$V_{PD(min)}$ (V)	14	14	14	35	35	35
$P_{PD(max)}$ (W)	1.23	3.2	8.4	7.7	20	52

104.4 Power Sourcing Equipment (PSE)

104.4.1 PSE types

Change 104.4.1 as follows:

For PoDL systems, there are multiple types of PSEs—Type A, Type B, Type C, ~~and~~ Type D, and Type E consistent with 104.1.3.

Insert the following new subclause (104.4.1a, including Table 104-1b) after 104.4.1:

104.4.1a PI pin assignments

A PSE provides power via a single two-wire connection. Table 104–1b in conjunction with Figure 104–3 illustrates the PSE pinout.

A PSE shall implement the PSE pinout in Table 104–1b.

Table 104–1b—PSE pinout

Contact	PI
1	PI+
2	PI–

104.4.3 PSE state diagram

104.4.3.3 Variables

Change the variable power_available as follows:

power_available

TRUE: a compatible PSE class to PD class pairing exists as defined in Table 104–2 and Table 104–2a, and the PSE is able to source the required voltage and power.

FALSE: a valid PSE class to PD class pairing does not exist as defined in Table 104–2 and Table 104–2a, or the PSE is not able to source the required voltage and power.

Change the title of Table 104-2 as follows:

Table 104–2—PSE power_available matrix for PSE and PD for classes 0 through 9

Insert the following new table (Table 104-2a) after Table 104-2:

Table 104–2a—PSE power_available matrix for PSE and PD for classes 10 through 15

			PSE Class[a]						
			Classes 0 to 9	30V reg			58V reg		
				10	11	12	13	14	15
PD Class[a]	Classes 0 to 9		See Table 104–2	—	—	—	—	—	—
	30V reg	10	—	x	x	x	—	—	—
		11	—	—	x	x	—	—	—
		12	—	—	—	x	—	—	—
	58V reg	13	—	—	—	—	x	x	x
		14	—	—	—	—	—	x	x
		15	—	—	—	—	—	—	x

[a]An ‘x’ denotes a valid PSE to PD Class pairing.

104.4.3.5 Functions

Change 104.4.3.5 as follows:

do_classification

This function returns the following variables:

CLASS_TYPE_INFO register:
~~The register contains 16 bits of information regarding the type and class of the PD.~~ Refer to Table 104–9 for a description of the contents.

VOLT_INFO register:
PSEs that support cable resistance measurement also return the VOLT_INFO register. Refer to Table 104–10 for a description of the contents.

POWER_INFO register:
PSEs that support cable resistance measurement also return the POWER_INFO register. Refer to Table 104–11 for a description of the contents.

POWER_ASSIGN register:
PSEs that support cable resistance measurement also return the POWER_ASSIGN register. Refer to Table 104–12 for a description of the contents.

104.4.4 PSE detection of a PD

104.4.4.1 Detection probe requirements

Change Table 104-3 as follows:

Table 104–3—PSE PI detection state electrical output requirements

Item	Parameter	Symbol	Unit	Min	Max	Type	Additional information
1	Open circuit voltage	V_{OC}	V	4.75	5.5	All	
2	Short-circuit current	I_{SC}	mA	—	24	All	
3	Valid test probe current	I_{valid}	mA	9	16	All	
4	Slew rate	I_{slew}	A/ms	—	1	All	
5	Output capacitance during detection	C_{out}	μF	—	2.64	A, B, C, D	
					0.4	E	
6	Maximum detection time	T_{det}	ms	—	3.11	All	See 104.4.4
7	Valid PD detection signature range measured at PSE PI	V_{good_PSE}	V	4.05	4.7	All	See 104.4.4.2

Table 104–3—PSE PI detection state electrical output requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Type	Additional information
8	Invalid PD detection signature high range measured at PSE PI	$V_{bad\_hi\_PSE}$	V	V_{oc}–0.05	—	All	See 104.4.4.3
9	Invalid PD detection signature low range measured at PSE PI	$V_{bad\_lo\_PSE}$	V	—	3.7	All	
10	Signature hold timer for validity	T_{sig_hold}	ms	1	—	All	See 104.4.4.2

104.4.6 PSE output requirements

Change Table 104-4 as follows (unchanged rows not shown):

Table 104–4—PSE output requirements

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
…								
3	Output slew rate dV/dt		V/ms	—	22	All	A, C	See 104.4.6.3
				—	2	All	E	See 104.4.6.3
				—	40	All	A, C, E	During inrush only
				—	200	All	B	See 104.4.6.3
…								
6	Short-circuit time limit	T_{LIM}	ms	10	75	~~All~~Classes 0 to 9	All	
				50	75	Classes 10 to 15		
7	Inrush time	T_{Inrush}	ms	3.17	3.87	~~All~~Classes 0 to 9	All	See 104.4.6.4
				50	75	Classes 10 to 15		
8	Classification time	T_{Class}	ms	—	366	~~All~~Classes 0 to 9	All	See 104.4.5
					1300	Classes 10 to 15		
…								

104.4.6.3 Power feeding ripple and transients

Change the text of 104.4.6.3 as follows (Figure 104-7 remains unchanged):

The ripple and transient limits specified in Table 104–4, items (4) and (3) respectively, are meant to preserve data integrity.

A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI of the PSE device under test (DUT) as shown in Figure 104-7. The input impedance, $Z_{in}(f)$, and transfer function, $H_1(f)$, of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PSE as specified by Table 104–4 item (4a), f_1 = 31.8 kHz ± 1%. When measuring the ripple voltage for a Type B PSE as specified in Table 104–4 item (4a), f_1 = 318 kHz ± 1%. When measuring the ripple voltage for a Type E PSE as specified in Table 104–4 item (4a), f_1 = 3.18 kHz ± 1%.

$$Z_{in}(f) = \left(100 \pm 0.1\,\% \times \frac{\sqrt{f^2 + {f_1}^2}}{f}\right)\Omega \quad (104\text{–}1)$$

$$H_1(f) = \frac{f}{\sqrt{f^2 + {f_1}^2}} \quad (104\text{–}2)$$

When measuring the ripple voltages for a Type A or Type C PSE as specified by Table 104–4 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 31.8 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 1 MHz ± 1%.

When measuring the ripple voltages for a Type B PSE as specified by Table 104–4 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 318 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%.

When measuring the ripple voltages for a Type E PSE as specified by Table 104–4 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 3.18 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 0.1 MHz ± 1%.

$$H_2(f) = \frac{f}{\sqrt{f^2 + {f_2}^2}} \quad (104\text{–}3)$$

104.5 Powered Device (PD)

104.5.1 PD types

Change 104.5.1 as follows:

For PoDL systems, there are ~~four~~five types of PDs—Type A, Type B, Type C, ~~and~~ Type D, and Type E consistent with 104.1.3.

Insert the following new subclause (104.5.1a, including Table 104-4a) after 104.5.1:

104.5.1a PD PI

A PD may receive power in two modes, Mode A and Mode B. Table 104–4a in conjunction with Figure 104–3 illustrates the PD pinout.

Table 104–4a—PD pinout

Contact	Mode A	Mode B
1	PI+	PI–
2	PI–	PI+

Class 0 to class 9 PDs shall be able to operate per the Mode A column in Table 104–4a. Class 10 to class 15 PDs shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the Mode A column and the Mode B column in Table 104–4a.

104.5.3 PD state diagram

104.5.3.5 Functions

Change 104.5.3.5 as follows:

do_sccp

This function returns the following variables to the PSE:

CLASS_TYPE_INFO register:
Rrefer to Table 104–9 for a description of the contents.

VOLT_INFO register:
PDs that support cable resistance measurement also return the VOLT_INFO register. Refer to Table 104–10 for a description of the contents.

POWER_INFO register:
PDs that support cable resistance measurement also return the POWER_INFO register. Refer to Table 104–11 for a description of the contents.

POWER_ASSIGN register:
PDs that support cable resistance measurement also return the POWER_ASSIGN register. Refer to Table 104–12 for a description of the contents.

104.5.6 PD power

Change Table 104-7 as follows (unchanged rows not shown):

Table 104–7—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD ~~t~~Type	Additional information
1	Input current dI/dt		A/ms	—	1	A, C	See 104.5.6.4
				—	10	B	
				—	0.1	E	
2	Input voltage dV/dt		V/ms	—	20	A, C	
				—	200	B	
				—	2	E	
…							
4f	Power supply turn on voltage (Classes 10, 11, and 12)	V_{On}	V	—	19.2	All	See 104.5.6.2
4g	Power supply turn on voltage (Classes 13, 14, and 15)			—	49		
…							
5f	Power supply turn off voltage (Classes 10, 11, and 12)	V_{Off}	V	11.2	—		
5g	Power supply turn off voltage (Classes 13, 14, and 15)			28	—		
…							
6b	Input capacitance during DO_CLASSIFICATION state	C_{IN_Class}	μF	—	0.2	~~All~~A, B, C, D	All classes
				—	0.4	E	
…							
7	Inrush enable delay time (Classes 0 to 9)	T_{power_dly}	ms	1.46	—	All	See 104.5.6.2
	Inrush enable delay time (Classes 10 to 15)			80			
…							
15	SCCP watchdog timeout	$T_{SCCP\_watch\text{-}dog}$	ms	150	200	~~All~~A, B, C, D	See 104.5.5
				1000	1300	E	

104.5.6.4 PD ripple and transients

Change the text of 104.5.6.4 as follows (Figure 104-9 remains unchanged):

The specifications for ripple and transients in Table 104–7 apply to the voltage or current at the PD PI generated by the PD circuitry. Ripple and transient limits are provided to preserve data integrity.

The PD DUT is connected to a power supply through a dc bias coupling network as shown in Figure 104-9. The ripple and transient specifications for a Type A or Type C PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Equation (96–12), and over the range of P_{PD}. The ripple and transient specifications for a Type B PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 97, and over the range of P_{PD}. The ripple and transient specifications for a Type E PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 146 and over the range of P_{PD}.

A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI. The input impedance, $Z_{in}(f)$, and transfer function, $H_1(f)$, of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PD as specified by Table 104–7 item (3a), f_1 = 31.8 kHz ± 1%. When measuring the ripple voltage for a Type B PD as specified by Table 104–7 item (3a), f_1 = 318 kHz ± 1%. When measuring the ripple voltage for a Type E PD as specified by Table 104–7 item (3a), f_1 = 3.18 kHz ± 1%.

When measuring the ripple voltages for a Type A or Type C PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where f_1 = 31.8 kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 1 MHz ± 1%. When measuring the ripple voltages for a Type B PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where f_1 = 318 kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%. When measuring the ripple voltages for a Type E PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where f_1 = 3.18 kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 0.1 MHz ± 1%.

104.6 Additional electrical specifications

104.6.2 Fault tolerance

Change the first paragraph in 104.6.2 as follows:

The PI for Type A, Type B, and Type C PSEs and PDs shall meet the fault tolerance requirements as specified in 96.8.3. The PI for Type E PSEs and PDs shall meet the fault tolerance requirements as specified in 146.8.5.

104.7 Serial communication classification protocol (SCCP)

Change 104.7 as follows:

Implementation of SCCP by PSEs and PDs that present a valid detection signature is optional. PDs that present an invalid detection signature as specified in Table 104–6 shall implement SCCP. The PSE acts as a master during the SCCP exchange, controlling the PD that acts as the slave device. SCCP is a current-sinking, wired-OR (e.g., open-drain or open-collector), half-duplex bidirectional serial data bus. The PSE sources the required pull-up current. ~~The logic high voltage is limited by the voltage signature device at the PD.~~ PDs can derive power from the PSE's pull-up current during classification via the PD PI.

Measurement of initial cable resistance, $R_{Cable\_initial}$, by PSEs and PDs that implement SCCP is optional. PSEs and PDs that implement cable resistance measurement support the VOLT_INFO, POWER_INFO, and POWER_ASSIGN registers (see Table 104–10, Table 104–11, and Table 104–12). PSEs that implement cable resistance measurement shall report assigned power through PoDL PSE Status 2 Register (see 45.2.9.3).

104.7.1 SCCP signaling

104.7.1.1 Initialization procedure—reset and presence pulses

Replace Figure 104-10 with the following figure:

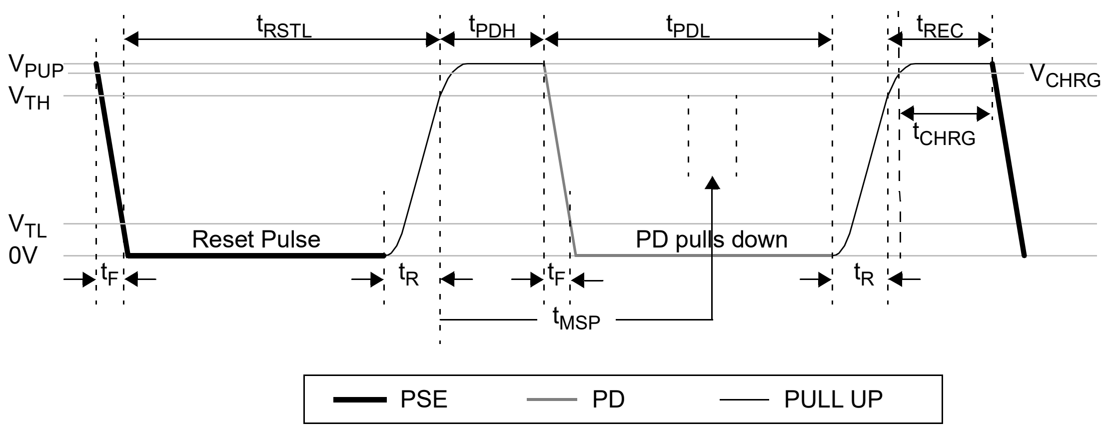


Figure 104–10—Reset command timing diagram

104.7.1.2 Write time slots

Change the first paragraph in 104.7.1.2 as follows:

There are two types of write time slots: Write 1 and Write 0 time slots. Figure 104–11 illustrates Write 0/1 timing diagrams. The PSE shall use a Write 1 time slot to transmit a logic 1 to the PD and a Write 0 time slot to transmit a logic 0 to the PD. All write time slots shall be $t_{WRITESLOT}$ in duration. The PSE shall initiate both types of write time slots by pulling V_{PSE} low.

Replace Figure 104-11 with the following figure:

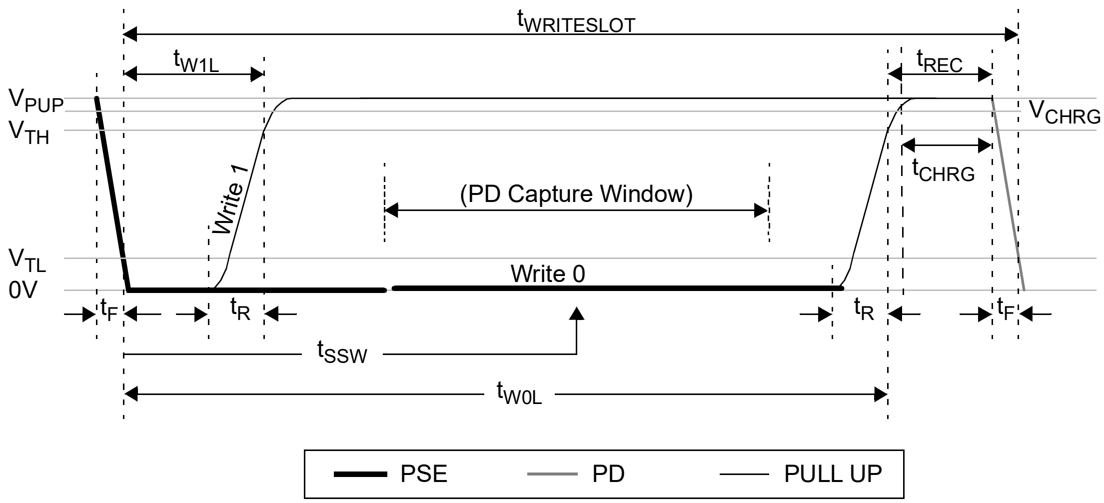


Figure 104–11—Write 0/1 slot timing diagram

104.7.1.3 Read time slots

Replace Figure 104-12 with the following figure:

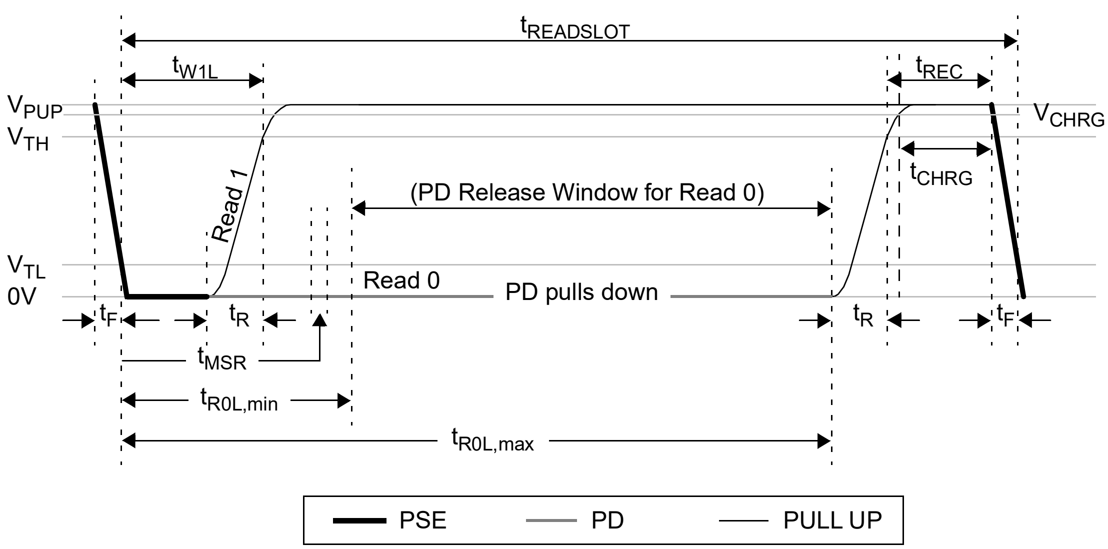


Figure 104–12—Read 0/1 slot timing diagram

Change the second paragraph in 104.7.1.3 as follows:

All read time slots shall be $t_{READSLOT}$ in duration. The PSE shall initiate a read time slot by pulling V_{PSE} low and then pulling-up V_{PSE} within t_{W1L}. After the PSE initiates the read time slot, the PD shall begin transmitting a 1 or 0 at its PI. The PD shall transmit a 1 by leaving V_{PD} high and transmit a 0 by pulling V_{PD} low. When transmitting a 0, the PD shall hold V_{PD} low and then release V_{PD} within t_{R0L}. V_{PSE} and V_{PD} will be pulled back to the high idle state by the PSE's pull-up current. Output data from the PD is valid for t_{MSR} after the falling edge that initiated the read time slot. Therefore, the PSE shall release V_{PSE} and then sample the subsequent voltage within t_{MSR} from the start of the read time slot SCCP electrical requirements.

Change Table 104-8 as follows:

Table 104–8—SCCP electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	PSE/PD Type	Additional information
1	PSE Pull-up Voltage (Classes 0 to 9)	V_{PUP}	V	$V_{good\_PSE\ max}$	5	All	See Table 104–3
	PSE Pull-up Voltage (Classes 10 to 15)				5.5		
2	PSE Pull-up Current	I_{PUP}	mA	9	16	All	
3	Input Logic High Voltage	V_{TH}	V	3	—	All	
4	Input Logic Low Voltage	V_{TL}	V	—	1	A, B, C, D, PSE/PD; E PD	
					2	E PSE	
5	Sink Current	I_L	mA	30	—	All	$V_{Port} > 0.8$ V
6a	Write Time Slot	$t_{WRITESLOT}$	ms	2.7	3.3	A, B, C, D	
				—	2.78	E	
6b	Read Time Slot	$t_{READSLOT}$	ms	2.7	3.3	A, B, C, D	
				—	3.83	E	
7	Recovery Time	t_{REC}	ms	0.27	0.33	All	
8	Write 0 Low Time	t_{W0L}	ms	1.8	2.2	All	
9	Write 1 Low Time	t_{W1L}	ms	0.08	0.25	A, B, C, D	
				0.09	0.61	E	
10	PD Sample Write Time	t_{SSW}	ms	0.5	1.5	A, B, C, D	
				0.77	1.43	E	
11	PSE Sample Read Time	t_{MSR}	ms	0.27	0.33	A, B, C, D	
				0.9	1.1	E	
12	Read 0 Low Time	t_{R0L}	ms	0.5	1.5	A, B, C, D	
				1.75	3.25	E	
13	Reset Time Low Time	t_{RSTL}	ms	9	11	A, B, C, D	
				8	10.5	E	

Table 104–8—SCCP electrical requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE/PD Type	Additional information
14	Presence-Detect High Time	t_{PDH}	ms	0.5	1.5	A, B, C, D	
				0.7	1.3	E	
15	Presence-Detect Low Time	t_{PDLOW}	ms	2.5	7.5	A, B, C, D	
				2.8	5.2	E	
				21	31	E	PDs that support link segment resistance measurement
16	PSE Sample Presence Time	t_{MSP}	ms	1.8	2.2	All	
17	Rise-Time	t_R	ms	0.025	0.105	A, B, C, D	
				0.025	0.5	E	
18	Fall-Time	t_F	ms	0.025	0.1	A, B, C, D	
				0.025	0.25	E	
19	Bus Capacitance	C_{BUS}	nF	—	6	A, B, C, D	
				—	80	E	
20	PD reservoir capacitor recharge voltage	V_{CHRG}	V	$0.9 \times V_{PUPmin}$	—	E	
21	PD reservoir capacitor recharge time	t_{CHRG}	ms	0.2	—	E	
22	Resistance margin factor	K_{RMF}	—	1.06	—	E	PSEs that support cable resistance measurement

Insert the following new subclauses [104.7.1.4 and 104.7.1.5, including Equation (104-4a), Equation (104-4b), and Equation (104-4c)] after 104.7.1.3:

104.7.1.4 Calculations for cable resistance

A PSE that implements cable resistance measurement may calculate cable resistance (dc loop resistance of the link segment) using the voltage and current at the PSE PI during the presence pulse and the voltage at the PD PI as shown in Equation (104–4a). The measurement tolerances in the voltage and current values should be included in the cable resistance measurement calculation. The initial calculated link segment cable resistance, $R_{Cable\_initial}$, is defined in Equation (104–4a).

$$R_{Cable\_initial} = \left(\frac{V_{PSE} - V_{Report\_PD}}{I_{PSE}}\right)\Omega \qquad (104\text{–}4a)$$

where

V_{Report_PD}	is the voltage at PD's PI during the presence pulse as reported in b[7:0] of VOLT_INFO in Table 104–10
V_{PSE}	is the voltage at PSE's PI during the presence pulse
I_{PSE}	is the current at PSE's PI during the presence pulse

The initial cable resistance value calculated in Equation (104–4a) is then margined by the Resistance Margin Factor, K_{RMF}, as shown in Equation (104–4b). The margined link segment cable resistance, R_{Cable}, should not exceed the maximum allowable link segment dc loop resistance for the class as shown in Equation (104–4b).

$$R_{Cable} = \min(R_{Cable\_initial} \times K_{RMF}, R_{Loop(max)})\,\Omega \qquad (104\text{–}4b)$$

where

$R_{Cable\_initial}$	is the initial calculated link segment cable resistance
K_{RMF}	is the Resistance Margin Factor per Table 104–8
$R_{Loop(max)}$	is the maximum allowable link segment dc loop resistance for the class per 104.2

104.7.1.5 Calculations for power allocation

A PD that supports cable resistance measurement may request a power allocation between 0.1 W and $P_{Class(max)}$ via the PD Requested Power, P_{PD_req}, field of the POWER_INFO register b[11:0]. The PD Requested Power may exceed $P_{PD(max)}$. A PSE that supports cable resistance measurement shall set PD Assigned Power (P_{PD_assign}) based on PD Requested Power, P_{PD_req}, and measured cable resistance as shown in Equation (104–4c):

$$P_{PD\_assign} = \left\{ \begin{array}{ll} \min(P_{PD\_req}, P_{Class(min)} - I_{PI(max)}{}^2 \times R_{Cable}) & \text{for } P_{PD\_\mathrm{req}} > P_{PD(max)} \\ P_{PD\_req} & \text{for } P_{PD\_\mathrm{req}} \le P_{PD(max)} \end{array} \right\} \mathrm{W} \qquad (104\text{–}4c)$$

where

P_{PD_req}	is the PD Requested Power as reported in b[11:0] of POWER_INFO in Table 104–11
P_{PD_assign}	is the PD Assigned Power by PSE as assigned in b[11:0] of POWER_ASSIGN in Table 104–12
$P_{Class(min)}$	see Table 104-1 for description

$I_{PI(max)}$ see Table 104-1 for description
$P_{PD(max)}$ see Table 104-1 for description

For systems that implement cable resistance measurement, the PSE determines P_{PD_assign}, as assigned in b[11:0] of POWER_ASSIGN in Table 104–12. Maximum average available power at the PD PI is P_{PD_assign}. P_{PD_assign} may be greater or less than $P_{PD(max)}$.

104.7.2 Serial communication classification protocols

Replace Figure 104-13 with the following figure (which includes VOLT_INFO, POWER_INFO read, POWER_ASSIGN write, and POWER_ASSIGN read commands):

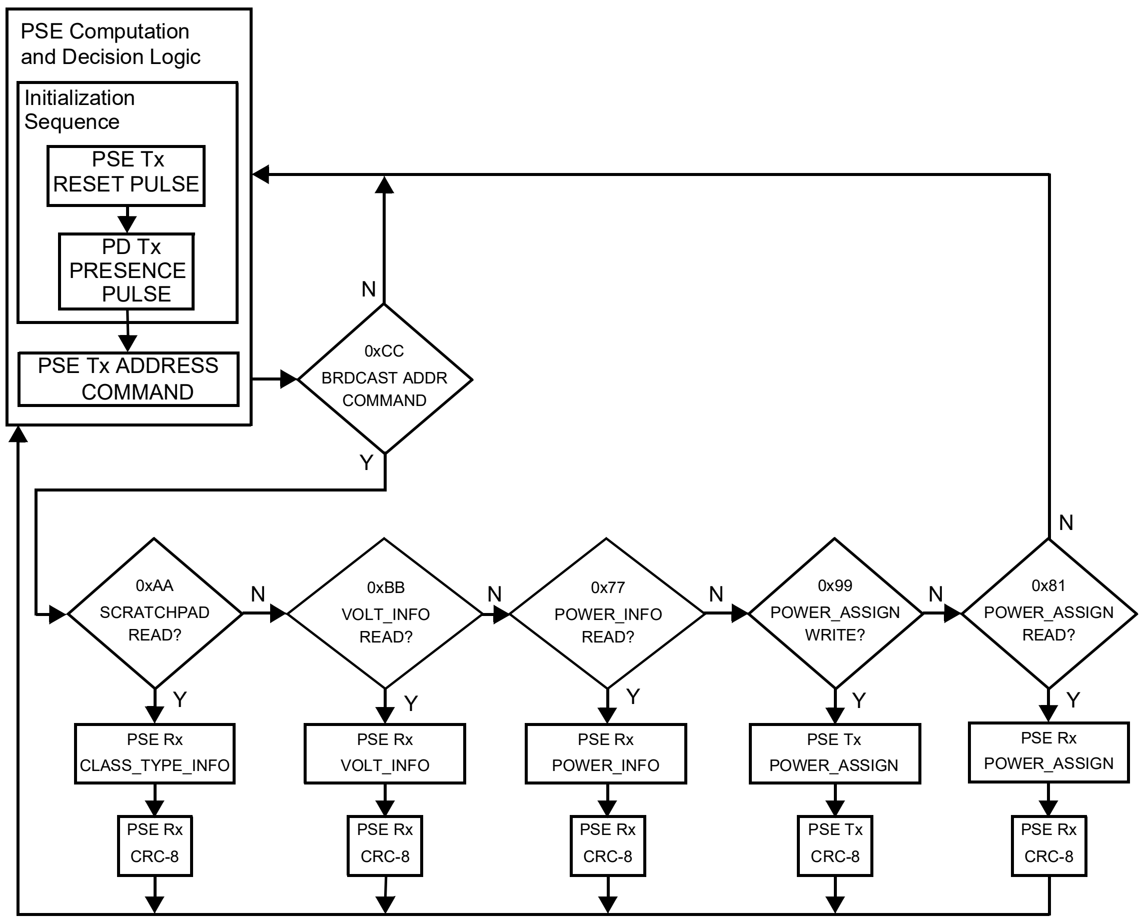


Figure 104–13—Address and Read_Scratchpad function command flowchart

104.7.2.4 Read_Scratchpad function command [0xAA]

Change Table 104-9 as follows:

Table 104–9—CLASS_TYPE_INFO register table

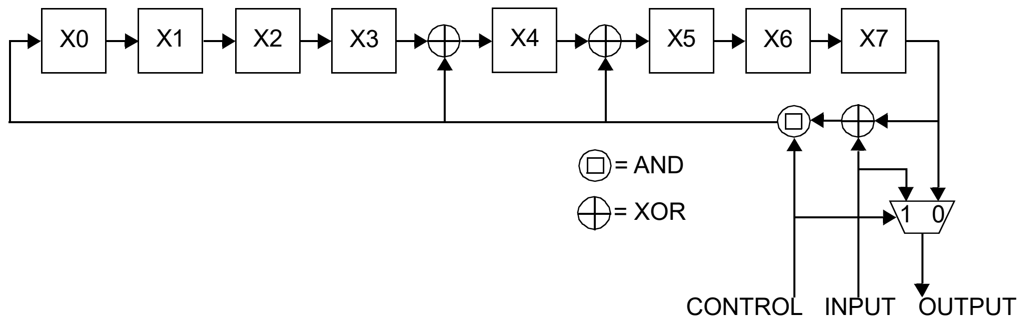
Bit(s)	Name	Description	R/W
b[15:12]	Type	15 14 13 12 1 1 1 0 = Type A 1 1 0 1 = Type B 1 0 1 1 = Type C 0 1 1 1 = Type D 1 1 0 0 = Type E	RO
b[11]	pd_faulted	1–error condition has occurred that prevented the PD from receiving power at the PI. Set to 1 when the pd_fault variable transitions from FALSE to TRUE 0–no error condition detected	RO/ LH
b[10]	~~Reserved~~ Cable resistance measurement	~~value always 0~~ 1 — Cable resistance measurement enabled 0 — Cable resistance measurement disabled	RO
b[9:0]	Class	9 8 7 6 5 4 3 2 1 0 1 1 1 1 1 1 1 1 1 0 =Class 0 1 1 1 1 1 1 1 1 0 1 =Class 1 1 1 1 1 1 1 1 0 1 1 =Class 2 1 1 1 1 1 1 0 1 1 1 =Class 3 1 1 1 1 1 0 1 1 1 1 =Class 4 1 1 1 1 0 1 1 1 1 1 =Class 5 1 1 1 0 1 1 1 1 1 1 =Class 6 1 1 0 1 1 1 1 1 1 1 =Class 7 1 0 1 1 1 1 1 1 1 1 =Class 8 0 1 1 1 1 1 1 1 1 1 =Class 9 0 0 0 0 0 0 0 0 0 1 =Class 10 0 0 0 0 0 0 0 0 1 0 =Class 11 0 0 0 0 0 0 0 0 1 1 =Class 12 0 0 0 0 0 0 0 1 0 0 =Class 13 0 0 0 0 0 0 0 1 0 1 =Class 14 0 0 0 0 0 0 0 1 1 0 =Class 15	RO

104.7.2.5 CRC8 field

Change the first paragraph 104.7.2.5 as follows:

The CRC8 field is an 8-bit cyclic redundancy check value. This value is computed as a function of the contents of the preceding ~~16-bit Scratchpad~~ Read/Write payload.

Change Figure 104-14 as follows (see changes in the CONTROL = 1 callout):



CONTROL = 1 when shifting the contents of ~~CLASS_TYPE_INFO~~ register
and calculating the CRC field

CONTROL = 0 when transmitting the CRC field

Figure 104–14—CRC8 field generation

Insert the following new subclauses (104.7.2.6 through 104.7.2.9, including Table 104–10, Table 104-11, and Table 104–12) after 104.7.2.5:

104.7.2.6 Read_VOLT_INFO command [0xBB]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_VOLT_INFO command. After receiving a Read_VOLT_INFO command, the PD shall respond with a 16-bit VOLT_INFO read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Read_VOLT_INFO command is shown in Figure 104–13. Table 104–10 illustrates the contents of the VOLT_INFO register.

Table 104–10—VOLT_INFO register table

Bit(s)	Name	Description	R/W[a]
b[15:8]	Reserved	Value always 0	RO
b[7:0]	Voltage at PD PI during Presence Pulse	± 20 mV tolerance, 10 mV per LSB	RO

[a]RO = Read only

104.7.2.7 Read_POWER_INFO command [0x77]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_INFO command. After receiving a Read_POWER_INFO command, the PD shall respond with a 16-bit POWER_INFO read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Read_POWER_INFO command is shown in Figure 104–13. Table 104–11 illustrates the contents of the POWER_INFO register.

Table 104–11—POWER_INFO register table

Bit(s)	Name	Description	R/W[a]
b[15:12]	Reserved	Value always 0	RO
b[11:0]	P_{PD_req} PD Requested Power	Power requested by PD, 0.025 W per LSB	RO

[a]RO = Read only

104.7.2.8 Write_POWER_ASSIGN command [0x99]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Write_POWER_ASSIGN command. After transmitting a Write_POWER_ASSIGN command, the PSE shall transmit a 16-bit POWER_ASSIGN write payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Write_POWER_ASSIGN command is shown in Figure 104–13. Table 104–12 illustrates the contents of the POWER_ASSIGN register.

Table 104–12—POWER_ASSIGN register table

Bit(s)	Name	Description	R/W[a]
b[15:12]	Reserved	Value always 0	RO
b[11:0]	P_{PD_assign} PD Assigned Power	PD assigned power, 0.025 W per LSB	R/W

[a]RO = Read only, R/W = Read/Write

104.7.2.9 Read_POWER_ASSIGN command [0x81]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_ASSIGN command. After receiving a Read_POWER_ASSIGN command, the PD shall respond with a 16-bit POWER_ASSIGN read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Read_POWER_ASSIGN command is shown in Figure 104–13. Table 104–12 illustrates the contents of the POWER_ASSIGN register.

Change the title of 104.9 as follows:

104.9 Protocol implementation conformance statement (PICS) proforma for Clause 104, Power over Data Lines (PoDL) of Single~~ Balanced Twisted~~-Pair Ethernet[8]

104.9.1 Introduction

Change the first paragraph of 104.9.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Clause 104, Power over Data Lines (PoDL) of Single~~ Balanced Twisted~~-Pair Ethernet, shall complete the following protocol implementation conformance statement (PICS) proforma.

104.9.2 Identification

104.9.2.2 Protocol summary

Change the protocol summary table as follows:

Identification of protocol standard	IEEE Std 802.3cg-2019, Clause 104 Power over Data Lines (PoDL) of Single~~ Balanced Twisted~~-Pair Ethernet
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cg-2019	

Date of Statement	

[8]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

104.9.3 Major capabilities/options

Insert the following new row at the beginning of the table in 104.9.3:

Item	Feature	Subclause	Value/Comment	Status	Support
*CRM	Implements cable resistance measurement functionality	104.7		SCCP:O	Yes [ ] No [ ] N/A [ ]

Insert the following new row after the *PSETC row in the table in 104.9.3:

Item	Feature	Subclause	Value/Comment	Status	Support
*PSETE	Implements PSE Type E functionality	104.1.3	Provides support for requirements of Type E Powered Sourcing Equipment	O	Yes [ ] No [ ]

Insert the following new row after the *PDTC row in the table in 104.9.3:

Item	Feature	Subclause	Value/Comment	Status	Support
*PDTE	Implements PD Type E functionality	104.1.3	Provides support for requirements of Type E Powered Device Equipment	O	Yes [ ] No [ ]

Change the title of 104.9.4 as follows:

104.9.4 PICS proforma tables for Clause 104, Power over Data Lines (PoDL) of Single~~ Balanced Twisted~~-Pair Ethernet

104.9.4.1 Link Segment

Change the table in 104.9.4.1 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
LNK1	DC loop resistance	104.2	Less than 6 Ω for ~~12 V unregulated classes~~Classes 0 and 1, ~~and~~ less than 6.5 Ω for Classes 2 through 9, less than 65 Ω for Classes 10 and 13, less than 25 Ω for Classes 11 and 14, less than 9.5 Ω for Classes 12 and 15~~12 V regulated, 24 V regulated and unregulated, and 48 V regulated classes~~	M	Yes [ ]

104.9.4.2 Power Sourcing Equipment (PSE)

Insert the following new row at the beginning of the table in 104.9.4.2:

Item	Feature	Subclause	Value/Comment	Status	Support
PSEa	PSE pinout	104.4.1a	See Table 104–1b	M	Yes [ ]

Insert the following new row at the end of the table in 104.9.4.2:

Item	Feature	Subclause	Value/Comment	Status	Support
PSE37	do_classification function for PSEs that support cable resistance measurement	104.4.3.5	Return VOLT_INFO, POWER_INFO, and POWER_ASSIGN registers	SCCP:O CRM:M	Yes [ ] No [ ] N/A [ ]

104.9.4.3 Powered Device (PD)

Insert the following new row at the beginning of the table in 104.9.4.3:

Item	Feature	Subclause	Value/Comment	Status	Support
PDa	PD PI	104.5.1a	Class 0 to 9 PDs operate per the Mode A column in Table 104–4a. Class 10 to 15 PDs are polarity-insensitive and are able to operate per Mode A and Mode B of Table 104–4a.	M	Yes [ ]

104.9.4.7 SCCP

Insert the following new rows at the end of the table in 104.9.4.7:

Item	Feature	Subclause	Value/Comment	Status	Support
SCCP29	8-bit Read_VOLT_INFO command	104.7.2.6	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP30	Reception of Read_VOLT_INFO function command	104.7.2.6	PD shall respond with a 16-bit VOLT_INFO read payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP31	8-bit Read_POWER_INFO command	104.7.2.7	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP32	Reception of Read_POWER_INFO function command	104.7.2.7	PD shall respond with a 16-bit POWER_INFO read payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
SCCP33	8-bit Write_POWER_ASSIGN command	104.7.2.8	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP34	Reception of Write_POWER_ASSIGN function command	104.7.2.8	PSE shall transmit a 16-bit POWER_ASSIGN write payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP35	8-bit Read_POWER_ASSIGN command	104.7.2.9	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP36	Reception of Read_POWER_ASSIGN function command	104.7.2.9	PD shall respond with a 16-bit POWER_ASSIGN read payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]

Insert Clause 146 to Clause 148 in numeric order (see later in this amendment for the addition of corresponding annexes):

146. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L

146.1 Overview

This clause defines the type 10BASE-T1L Physical Coding Sublayer (PCS) and type 10BASE-T1L Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 10BASE-T1L Physical Layer (PHY). Provided in this clause are functional and electrical specifications for the type 10BASE-T1L PCS, PMA, and MDI. 10BASE-T1L does not define an AUI.

The 10BASE-T1L PHY is a full-duplex PHY specification, capable of operating at 10 Mb/s. The 10BASE-T1L PHY is intended to be operated over a single balanced pair of conductors, defined in 146.7. The cabling supporting the operation of the 10BASE-T1L PHY is defined in terms of performance requirements between the DTE attachment points [Medium Dependent Interface (MDI)], allowing implementers to provide their own cabling to operate the 10BASE-T1L PHY as long as the normative requirements included in this clause are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 10BASE-T1L PHY that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

146.1.1 Relationship of 10BASE-T1L to other standards

The relationship between the 10BASE-T1L PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet model are shown in Figure 146–1. The PHY sublayers (shown shaded) in Figure 146–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 10BASE-T1L is defined in Clause 98. MII is defined in Clause 22.

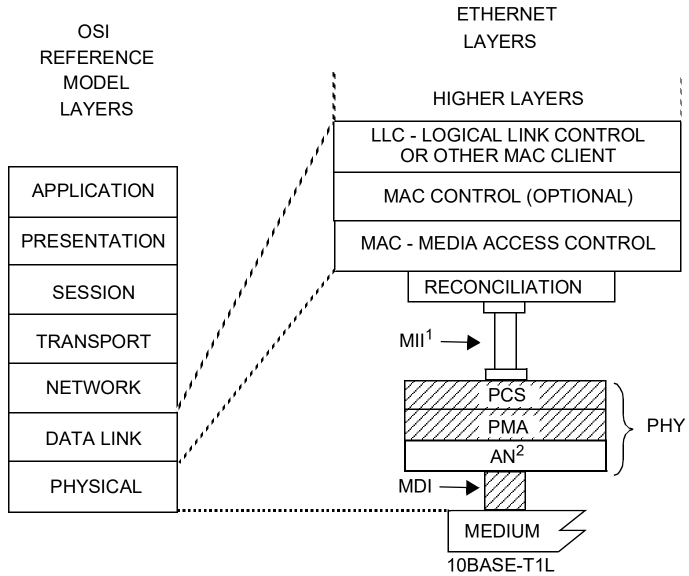
146.1.2 Operation of 10BASE-T1L

The 10BASE-T1L PHY operates using full-duplex communications over a single balanced pair of conductors with an effective data rate of 10 Mb/s in each direction simultaneously. The PHY supports operation on a link segment supporting up to ten in-line connectors using a single balanced pair of conductors for up to at least 1000 meters.

The 10BASE-T1L PHY utilizes 3-level Pulse Amplitude Modulation (PAM3) transmitted at 7.5 MBd on the link segment. A 33-bit scrambler is used to improve the EMC performance. MII TXD<3:0>, TX_EN, and TX_ER are encoded together using 4B3T encoding, where 4B3T encoding is used to keep the running average (DC baseline) of the transmitted PAM3 symbols within bounds. The PAM3 mapping, scrambler, and 4B3T encoder/decoder are all contained in the PCS (see 146.3).

The 10BASE-T1L PHY may optionally support an increased transmit and receive capability, supporting 2.4 Vpp differential. See 146.5.4.1.

Auto-Negotiation may be used by 10BASE-T1L devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

NOTE 1—MII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 146–1—Relationship of 10BASE-T1L PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

A 10BASE-T1L PHY optionally supports Energy-Efficient Ethernet (see Clause 78) and advertises the EEE capability during Auto-Negotiation as described in Annex 98B.3. The EEE capability is a mechanism by which 10BASE-T1L PHYs are able to reduce power consumption during periods of low link utilization.

A 10BASE-T1L PHY is capable of operating both as MASTER or SLAVE, with one mode active as determined according to 146.6.2. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the MASTER-SLAVE relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If Auto-Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of the PHYs. The MASTER and SLAVE are synchronized by a PMA Clock Recovery function (see 146.4.6).

The 10BASE-T1L PMA couples messages from the PCS to the MDI and provides clock recovery, link management, and PHY Control functions. The PMA provides full duplex communications at 7.5 MBd over a single balanced pair of conductors. PMA functionality is described in 146.4. The MDI is specified in 146.8.

146.1.2.1 Physical Coding Sublayer (PCS)

The 10BASE-T1L PCS couples a Media Independent Interface (MII), as described in Clause 22, to the 10BASE-T1L Physical Medium Attachment (PMA) sublayer.

146.1.2.2 Physical Medium Attachment (PMA) sublayer

The 10BASE-T1L PMA couples messages from the PCS service interface onto a single balanced pair of conductors and supports the link management and the 10BASE-T1L PHY Control function. The PMA provides full duplex communications over a single balanced pair of conductors up to 1000 m in length.

146.1.2.3 EEE capability

A 10BASE-T1L PHY optionally supports the EEE capability, as described in 78.3. The EEE capability is a mechanism by which 10BASE-T1L PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter the LPI mode of operation after completing training. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. The transition to or from LPI mode does not cause any MAC frames to be lost or corrupted.

In the transmit direction, the transition to the LPI transmit mode begins when the PCS transmit function detects an "Assert Low Power Idle" condition on the MII. If this condition is detected, tx_lpi_active is set true and shortly after this the PHY asserts the loc_lpi signal, which is transmitted within the IDLE symbol stream to the remote PHY. This sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. After the transmission of the sleep indications, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode, the PHY may cease transmission to save power and the link partner may disable receiver functions to save additional power. Periodically, the transmit function of the local PHY enters a refresh mode during which idle transmission resumes, and this may be used by the link partner to update adaptive filters and timing recovery circuits. Alternation between LPI quiet and refresh transmit modes proceeds according to a synchronized process between the PHYs, independent of data traffic patterns at the MII. The quiet-refresh cycling continues until the PCS function detects a condition that is not Assert Low Power Idle on the MII. This condition signals to the PHY that the LPI transmit mode should end. The PHY transmits an IDLE symbol stream with loc_lpi de-asserted, indicating to the remote PHY that the local PHY is back to normal transmit mode.

Support for EEE capability is advertised during Auto-Negotiation. See Annex 98B.3 for details. Transitions to and from the LPI transmit mode are controlled via MII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep and wake signaling.

146.1.2.4 Signaling

10BASE-T1L signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over a single balanced pair of conductors. The signaling scheme achieves a number of objectives including the following:

a) Algorithm mapping and inverse mapping from nibble data to ternary symbols and back.
b) Uncorrelated symbols in the transmitted symbol stream.
c) No correlation between symbol streams traveling both directions.
d) Ability to rapidly or immediately determine if a symbol stream represents data or idle.
e) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
g) Optionally, ability to signal to the remote PHY that the transmitting PHY is entering the LPI mode or exiting the LPI mode and returning to normal power operation.

146.1.3 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

146.1.3.1 State diagram notation

The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE, all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE, the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

146.1.3.2 State diagram timer specifications

All timers operate in the manner described in 40.4.5.2.

146.1.3.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

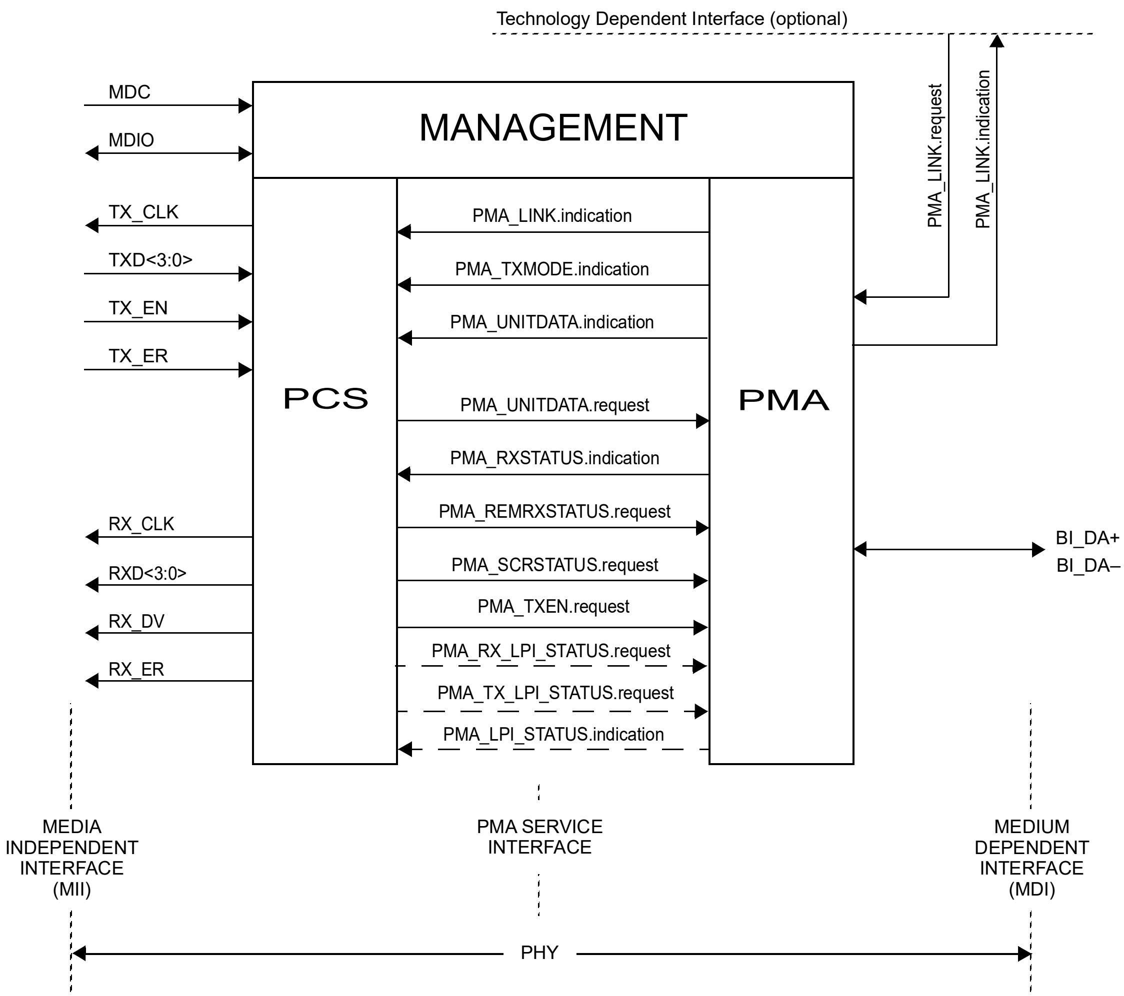
146.2 Service primitives and interfaces

The 10BASE-T1L PHY uses the service primitives and interfaces in 40.2, with exception of the following clarifications and differences noted in this subclause, in support of 10 Mb/s operations over a single balanced pair of conductors. Figure 146–2 shows the relationship of the service primitives and interfaces used by the 10BASE-T1L PHY.

The 10BASE-T1L PHY uses the Media Independent Interface (MII) as specified in Clause 22. The optional Technology Dependent Interface is used for Auto-Negotiation and is described in 98.4.

As shown in Figure 146–2, 10BASE-T1L uses the following service primitives to exchange symbol vectors, status indications, and control signals across the PMA service interface:

PMA_LINK.request (link_control)
PMA_LINK.indication (link_status)
PMA_TXMODE.indication (tx_mode)
PMA_UNITDATA.indication (rx_symb_vector)
PMA_UNITDATA.request (tx_symb_vector)
PMA_RXSTATUS.indication (loc_rcvr_status)
PMA_REMRXSTATUS.request (rem_rcvr_status)
PMA_SCRSTATUS.request (scr_status)
PMA_TXEN.request (tx_enable_mii)
PMA_RX_LPI_STATUS.request (rx_lpi_active)
PMA_TX_LPI_STATUS.request (tx_lpi_active)
PMA_LPI_STATUS.indication (loc_lpi)



NOTE—Service interface primitives shown with dashed lines are required only for EEE capability.

Figure 146–2—10BASE-T1L PHY interfaces

146.2.1 PMA_LINK.request

This primitive allows the Auto-Negotiation or the PHY Link Synchronization algorithm to enable and disable operation of the PMA, as specified in 98.4.2.

146.2.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of the following two values:

DISABLE:	Used by the Auto-Negotiation function to disable the PHY.
ENABLE:	Used by the Auto-Negotiation function to enable the PHY.

146.2.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

146.2.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 146.4.4 and the PMA Link Monitor function as described in 146.4.5.

146.2.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the Auto-Negotiation functions about the status of the underlying link.

146.2.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on the following two values:

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 10BASE-T1L link is established. Reliable reception of signals transmitted from the remote PHY is possible.

146.2.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 146–18.

146.2.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

146.2.3 PMA_TXMODE.indication

The transmitter in a 10BASE-T1L link normally sends symbols over the MDI that represent an MII data stream with framing, scrambling and encoding of data, control information, or idles.

146.2.3.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

The PMA_TXMODE.indication specifies to PCS Transmit, via the parameter tx_mode, what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted during transmission of sequences of symbols representing an MII data stream in the data mode.
SEND_I	This value is continuously asserted when transmission of sequences of idle symbols is to take place.
SEND_Z	This value is continuously asserted when transmission of sequences of zeros is required.

146.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

146.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 146.3.3.

146.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb_vector parameter from the PMA to the PCS.

146.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception, the PMA_UNITDATA.indication conveys to the PCS, via the parameter rx_symb_vector, the value of symbols detected on the MDI during each cycle of the recovered clock.

146.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication (rx_symb_vector) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 7.5 MHz, as governed by the recovered clock.

146.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

146.2.5 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb_vector parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 146.3.3 to represent MII data, idle data, or zero data.

146.2.5.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA, via the parameter tx_symb_vector, the value of the symbols to be sent over the MDI. The tx_symb_vector may take on one of the values in the set {–1, 0, +1}.

146.2.5.2 When generated

The PCS generates PMA_UNITDATA.request (tx_symb_vector) synchronously with every transmit clock cycle.

146.2.5.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with optional transmit filtering and other specified PMA Transmit processing.

146.2.6 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Receive and PMA PHY Control function the information on whether the status of the overall receive link is satisfactory or not. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting disparity errors during reception of the symbol stream.

146.2.6.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the following form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

146.2.6.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

146.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 146.3.3.4.3 and 146.3.4.

146.2.7 PMA_REMRXSTATUS.request

This primitive is generated by PMA Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received within the idle data stream of the remote PHY.

146.2.7.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the following form:

OK	The receive link of the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

146.2.7.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in the idle data received from the remote PHY.

146.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in 146.4.4.

146.2.8 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

146.2.8.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values of the following form:

OK	The descrambler has achieved synchronization.
NOT_OK	The descrambler is not synchronized.

146.2.8.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

146.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–15.

146.2.9 PMA_TXEN.request (tx_enable_mii)

This primitive is generated by PCS Data Transmission Enable function to communicate the status of the tx_enable_mii signal to the PMA. The parameter tx_enable_mii conveys to the PMA PHY Control function the information about the actual data transmission status.

146.2.9.1 Semantics of the primitive

PMA_TXEN.request (tx_enable_mii)

The tx_enable_mii parameter can take on one of two values of the following form:

TRUE	Transmission is enabled.
FALSE	Transmission is disabled.

146.2.9.2 When generated

PCS Data Transmission Enable function generates PMA_TXEN.request messages to indicate a change in tx_enable_mii variable.

146.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–15.

146.2.10 PMA_RX_LPI_STATUS.request (rx_lpi_active)

When the PHY supports the EEE capability, this primitive is generated by the PCS receive function to indicate the status of the receive link of the local PHY. The parameter PMA_RX_LPI_STATUS.request conveys to the PMA receive function and the PMA PHY control function information regarding whether the PCS receive function is in the LPI receive mode.

146.2.10.1 Semantics of the primitive

PMA_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the following form:

TRUE	The PCS receive function is in the LPI receive mode.
FALSE	The PCS receive function is not in the LPI receive mode.

146.2.10.2 When generated

The PCS generates PMA_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in Figure 146–9 and Figure 146–10.

146.2.10.3 Effect of receipt

The receiver may adjust the clock recovery while being in low power idle mode. Additionally, checking of the descrambler status in the PHY control state diagram is suppressed, as the receiver is disabled.

146.2.11 PMA_TX_LPI_STATUS.request (tx_lpi_active)

When the PHY supports the EEE capability, this primitive is generated by the PCS transmit function to indicate the status of “Assert Low Power Idle” on the MII. The parameter PMA_TX_LPI_STATUS.request conveys to the PMA control function information regarding whether the PCS transmit function is receiving “Assert Low Power Idle” on the MII.

146.2.11.1 Semantics of the primitive

PMA_TX_LPI_STATUS.request (tx_lpi_active)

The tx_lpi_active parameter can take on one of two values of the following form:

TRUE	The PCS transmit function is receiving “Assert Low Power Idle” on the MII.
FALSE	The PCS transmit function is not receiving “Assert Low Power Idle” on the MII.

146.2.11.2 When generated

The PCS generates PMA_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable to the PMA PHY control function. Tx_lpi_active is set to true if “Assert Low Power Idle” is received from the MII; otherwise, it is set to false.

146.2.11.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–15 and Figure 146–17.

146.2.12 PMA_TX_LPI_STATUS.indication

When the PHY supports the EEE capability, this primitive is generated by the PMA PHY control function to indicate a sleep or wake event. The parameter PMA_TX_LPI_STATUS.indication conveys to the PCS transmit function information regarding whether the PHY should indicate a sleep or a wake event to the remote PHY.

146.2.12.1 Semantics of the primitive

PMA_TX_LPI_STATUS.indication (loc_lpi)

The loc_lpi parameter can take on one of two values of the following form:

TRUE	Communicate to the remote PHY that LPI mode will be entered by the local PHY.
FALSE	Communicate to the remote PHY that normal IDLE mode will be entered by the local PHY.

146.2.12.2 When generated

The PMA generates PMA_TX_LPI_STATUS.indication messages to indicate a change in the loc_lpi variable.

146.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 146.3.3.4.3.

146.3 Physical Coding Sublayer (PCS) functions

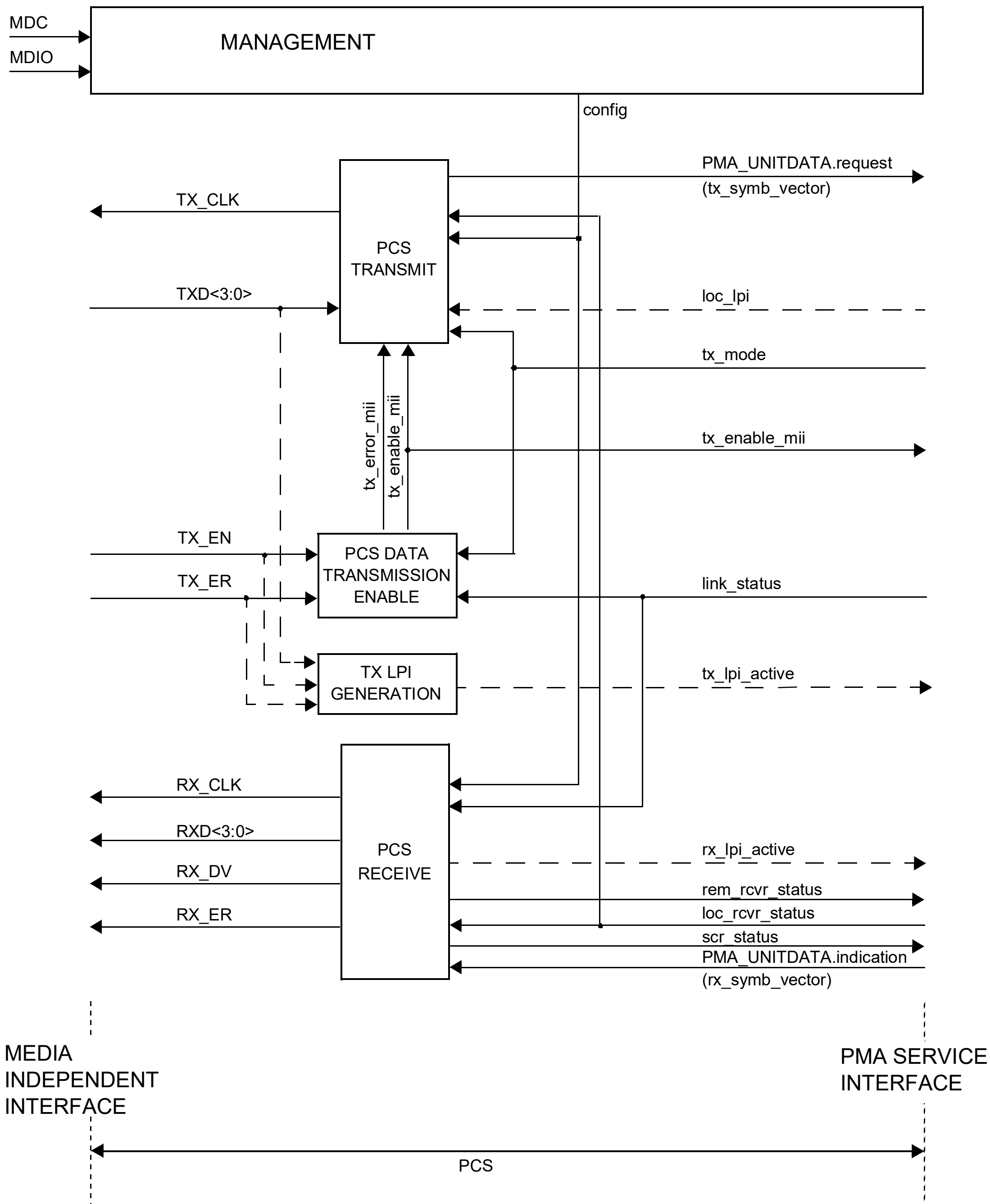
The Physical Coding Sublayer (PCS) consists of PCS Reset, the PCS Data Transmission Enable, PCS Transmit, and PCS Receive functions as shown in Figure 146–3. The PCS Reset function is explained in 146.3.1, the PCS Data Transmission Enable function is explained in 146.3.2, the PCS Transmit function is explained in 146.3.3, the PCS Receive function is explained in 146.3.4, and the PCS Loopback function is explained in 146.3.5.

146.3.1 PCS Reset function

PCS reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset shall set pcs_reset = TRUE while any of the above reset conditions holds true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.



NOTE—Signals shown with dashed lines are required only for EEE capability.

Figure 146–3—PCS reference diagram

146.3.2 PCS Data Transmission Enable

The PCS Data Transmission Enable function shall conform to the PCS data transmission enabling state diagram in Figure 146–4. When tx_mode is equal to SEND_N, the signals tx_enable_mii and tx_error_mii are equal to the values of the MII signals TX_EN and TX_ER respectively; otherwise, tx_enable_mii and tx_error_mii are set to the value FALSE.

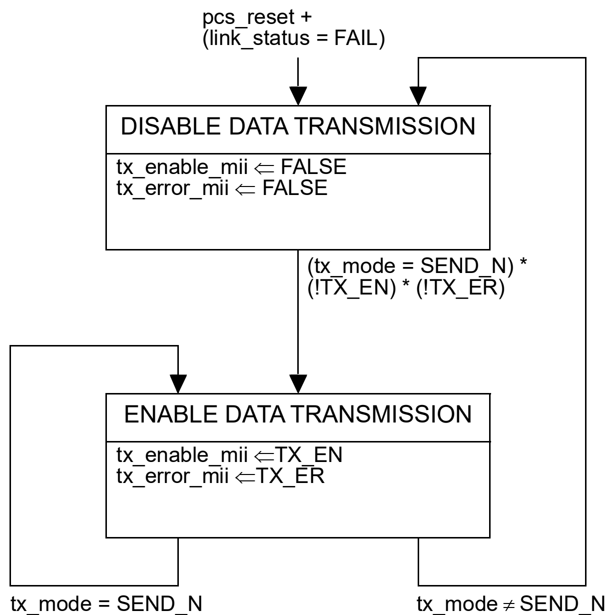


Figure 146–4—PCS data transmission enabling state diagram

146.3.2.1 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

tx_enable_mii
: The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4. When this variable is set to FALSE transmission is disabled, when set to TRUE transmission is enabled.
Values: TRUE or FALSE

tx_error_mii
: The tx_error_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

TX_EN
The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER
The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode
The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

146.3.3 PCS Transmit

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 146–5 (see 146.3.3.1.6) and the PCS Transmit multiplexer state diagram in Figure 146–6 (see 146.3.3.2.4) and to the associated state variables, functions, timers, and messages.

146.3.3.1 PCS Transmit state diagram

Upon the assertion of TX_EN, the PCS Transmit state diagram passes an SSD of 4 code-groups to the PMA, which replaces the first 2 bytes of the preamble. Following SSD, TXD[3:0] is encoded into ternary symbols using encoding rules, specified in 146.3.3.5.1, until TX_EN is de-asserted.

Following the de-assertion of TX_EN, a special code ESD (or ERR_ESD when a transmit error is encountered, which means that TX_ER was high at any point during the transmission) of 4 code-groups is generated, after which the transmission of idle mode according to 146.3.3.5.1 is resumed.

10BASE-T1L has one special code-group {0, 0, 0} that is not used by Idle or Data symbols. This code-group is used for the COMMA symbols within the delimiters. See Figure 146–5 for more details.

The 10BASE-T1L PHY supports normal operation and link training operation. In training operation, the PCS ignores signals from the MII and sends only the idle signals to the PMA until the training process is complete.

If tx_mode has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA.

If tx_mode has the value SEND_I, PCS Transmit generates sequences of symbols according to the encoding rule in idle mode as described in 146.3.3.5.1.

If tx_mode has the value SEND_N, PCS Transmit generates symbols A_n at each symbol period representing data, special control symbols like SSD/ESD, or IDLE symbols as defined in 146.3.3.5.1. The transition from idle to data is signaled by an SSD and the end of transmission of data is signaled by an ESD.

During training operation (when tx_mode is SEND_I), knowledge of the transmitted symbols may be used at the receiver side to perform any signal conditioning necessary for meeting the required performance during normal operation. When the link is up, the PHY enters SEND_N mode and the transmitted PAM3 symbols are used at the receiver PHY for continued clock frequency/phase tracking.

146.3.3.1.1 Variables

error

PCS local variable that records if an errored transmission has occured during data transmission.
Values: TRUE or FALSE

pcs_reset

The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

tx_enable_mii

The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4. When this variable is set to FALSE transmission is disabled, when set to TRUE transmission is enabled.
Values: TRUE or FALSE

tx_error_mii

The tx_error_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

tx_mode

The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

loc_rcvr_status

The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

loc_lpi

The variable loc_lpi is set by the PHY Control function in the PMA to indicate that it has entered low power idle mode.
Values: TRUE or FALSE

Sy_n[4:0]

The Sy_n[4:0] bits from the scrambler as defined in 146.3.3.4.2.

Sd_n[3:0]

The Sd_n[3:0] signal of the scrambler output as defined in 146.3.3.4.3.

Tx_n

Alias for tx_symb_vector at time n.

tx_code_group {TA_n, TB_n, TC_n}

A triplet of ternary symbols generated by the PCS Transmit state diagram. These include 4B3T encoded data and assigned values (see 146.3.3.5). The element TA_n is the first ternary symbol transmitted; TC_n is the last ternary symbol transmitted.
Value: A triplet of ternary transmit symbols. Each of the ternary symbols may take on one of the values {–1, 0, +1}.

tx_disparity

PCS local variable containing the running disparity. After PCS Reset, the initial value shall be set to 2.
Values: 1 to 4, depending on running disparity.

146.3.3.1.2 Functions

ENCODE

In the PCS Transmit process, this function takes as its arguments $Sd_n[3:0]$ and the tx_disparity and returns the corresponding tx_code_group as well as the updated tx_disparity. ENCODE follows the 4B3T rules defined in 146.3.3.5.1.

$$\{tx\_code\_group,\ tx\_disparity\} = ENCODE(Sd_n[3:0],\ tx\_disparity)$$

The tx_disparity can be between 1 and 4 and the respective tx_code_group is taken from the 4B3T encoding rules defined in Table 146–1 based on the $Sd_n[3:0]$ value and the tx_disparity:

$$tx\_code\_group = table_{4B3T}(Sd_n[3:0],\ tx\_disparity)$$

The second output value of this function is an updated tx_disparity value, which is calculated in the following way:

$$tx\_disparity = tx\_disparity + \text{disparity of currently encoded } tx\_code\_group$$

DISPRES

The function DISPRES returns one of the eight possible DISPRESET3 values for tx_code_group (see Table 146–2), depending on the values of $Sy_n[4]$ and tx_disparity:

$$tx\_code\_group = table_{DISPRESET3}(Sy_n[4],\ tx\_disparity)$$

RND_SSD4

The function RND_SSD4 takes $Sy_{n-1}[4]$ as its argument and returns the corresponding tx_code_group as well as the updated tx_disparity.

$$\{tx\_code\_group,\ tx\_disparity\} = RND\_SSD4(Sy_{n-1}[4])$$

The returned tx_code_group corresponds to one of the two possible SSD4 code-groups (see Table 146–3), depending on the value of $Sy_{n-1}[4]$:

$$tx\_code\_group = table_{SSD4}(Sy_{n-1}[4])$$

The returned tx_disparity also depends on the value of $Sy_{n-1}[4]$ as follows:

$$tx\_disparity = \begin{cases} 2, & \text{if } Sy_{n-1}[4] = 0 \\ 3, & \text{otherwise} \end{cases}$$

RND_ESD4

The function RND_ESD4 takes $Sy_{n-1}[4]$ as its argument and returns the corresponding tx_code_group as well as the updated tx_disparity.

$$\{tx\_code\_group,\ tx\_disparity\} = RND\_ESD4(Sy_{n-1}[4])$$

The returned tx_code_group corresponds to one of the two possible ESD4 code-groups (see Table 146–3), depending on the value of $Sy_{n-1}[4]$:

$$tx\_code\_group = table_{ESD4}(Sy_{n-1}[4])$$

The returned tx_disparity also depends on the value of $Sy_{n-1}[4]$ as follows:

$$tx\_disparity = \begin{cases} 2, & \text{if } Sy_{n-1}[4] = 0 \\ 3, & \text{otherwise} \end{cases}$$

RND_ESD_ERR4

The function RND_ESD_ERR4 takes $Sy_{n-1}[4]$ as its argument and returns the corresponding tx_code_group as well as the updated tx_disparity.

$$\{tx\_code\_group, tx\_disparity\} = RND\_ESD\_ERR4(Sy_{n-1}[4])$$

The returned tx_code_group corresponds to one of the two possible ESD_ERR4 code-groups (see Table 146–3), depending on the value of $Sy_{n-1}[4]$:

$$tx\_code\_group = table_{ESD\_ERR4}(Sy_{n-1}[4])$$

The returned tx_disparity also depends on the value of $Sy_{n-1}[4]$ as follows:

$$tx\_disparity = \begin{cases} 2, \text{ if } Sy_{n-1}[4] = 0 \\ 3, \text{ otherwise} \end{cases}$$

146.3.3.1.3 Timers

symb_triplet_timer

A continuous free-running timer that shall expire synchronously with every third expiration of symb_timer. TX_CLK (see 22.2.2.1) shall be generated from symb_triplet_timer with the rising edge of TX_CLK generated synchronously with symb_triplet_timer_done.
Restart time: Immediately after expiration; restarting the timer resets the condition symb_triplet_timer_done.
Duration: Three symbol times (see 146.5.4.5)

146.3.3.1.4 Abbreviations

STD

Alias for symb_triplet_timer_done.

146.3.3.1.5 Constants

COMMA

A vector of three ternary symbols in the first or second code-group of any delimiter as specified in 146.3.3.5.1.

ZERO

A vector of three zero symbols sent when tx_mode = SEND_Z as specified in 146.3.3.5.2.

146.3.3.1.6 State diagram

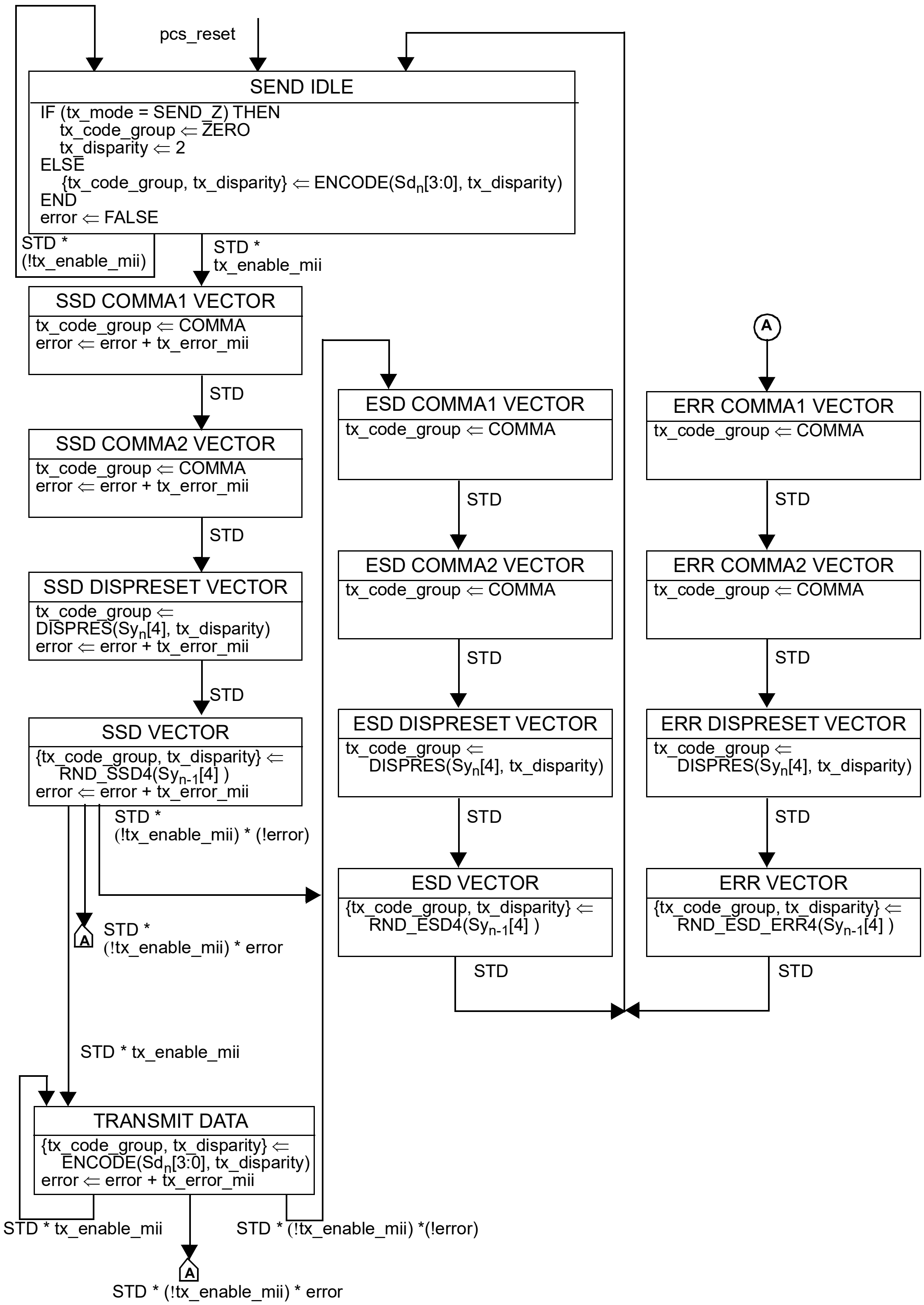


Figure 146–5—PCS Transmit state diagram

146.3.3.2 PCS Transmit multiplexer state diagram

In each symbol period, the PCS Transmit multiplexer generates a ternary symbol that can take the values of {–1, 0, +1} and passes it to the PMA sublayer via the PMA_UNITDATA.request primitive. The nominal symbol clock frequency is specified in 146.5.4.5.

146.3.3.2.1 Variables

pcs_reset

The pcs_reset parameter set by the PCS reset function.
Values: TRUE or FALSE

tx_symb_vector

A ternary symbol generated through serialization of tx_code_group. This symbol is conveyed to the PMA as the parameter of a PMA_UNITDATA.request(tx_symb_vector) service primitive.
Values: A ternary transmit symbol. The ternary symbol may take on one of the values {–1, 0, +1}.

tx_code_group $\{TA_n, TB_n, TC_n\}$

A triplet of ternary symbols generated by the PCS Transmit state diagram. The element TA_n is the first ternary symbol transmitted; TC_n is the last ternary symbol transmitted.
Value: A triplet of ternary transmit symbols. Each of the ternary symbols may take on one of the values {–1, 0, +1}.

146.3.3.2.2 Timers

symb_timer

A continuous free-running timer. The symb_timer expires when the PMA_UNITDATA.request is serviced, synchronously with TX_TCLK.
Continuous timer: The condition symb_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration; restarting the timer resets the condition symb_timer_done.
Duration: One symbol time (see 146.5.4.5)

146.3.3.2.3 Abbreviations

PUDR

Alias for PMA_UNITDATA.request(tx_symb_vector).

146.3.3.2.4 State diagram

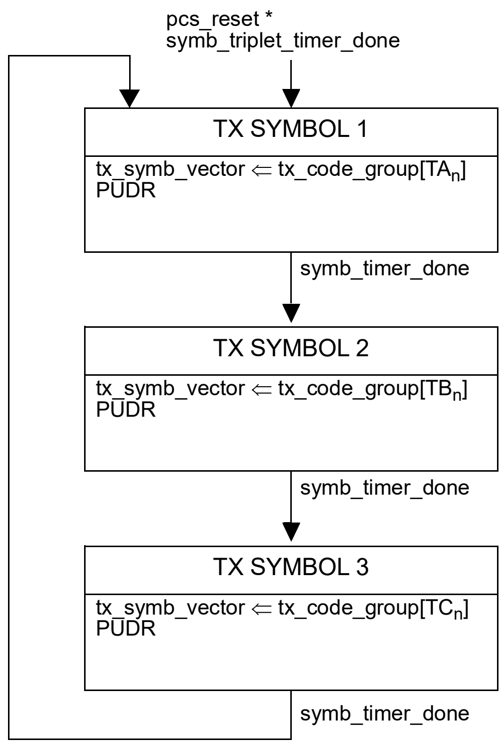


Figure 146–6—TX multiplexer state diagram

146.3.3.3 PCS Transmit symbol generation

The reference diagram of transmit symbol generation is indicated in Figure 146–7. The tx_code_group is the code-group $\{TA_n, TB_n, TC_n\}$.

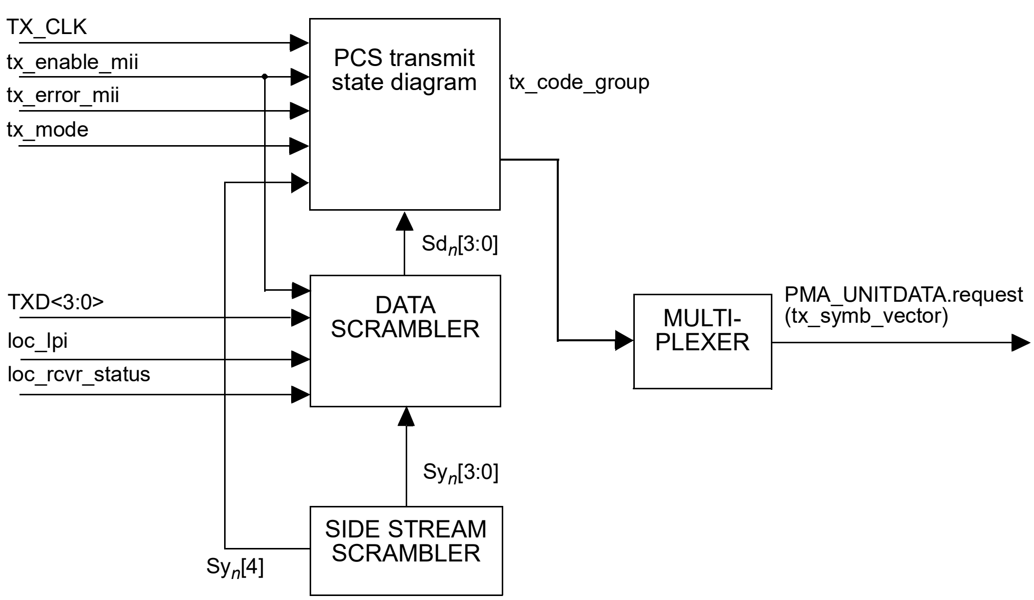


Figure 146–7—PCS transmit symbol generation

146.3.3.4 Data and idle stream scrambling

The scrambled bits $Sd_n[3:0]$ used by the ENCODE function defined in 146.3.3.1.2 are generated as follows.

146.3.3.4.1 Side-stream scrambler polynomial

The PCS Transmit function shall employ side-stream scrambling. For the master PHY, PCS Transmit shall employ

$$g_m(x) = 1 + x^{13} + x^{33} \quad (146\text{–}1)$$

as transmitter side-stream scrambler generator polynomial. For the slave PHY, PCS Transmit shall employ

$$g_s(x) = 1 + x^{20} + x^{33} \quad (146\text{–}2)$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream generator polynomials by linear-feedback shift registers is shown in Figure 146–8. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each tx_code_group period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. The scrambler state shall not be initialized to all zeros.

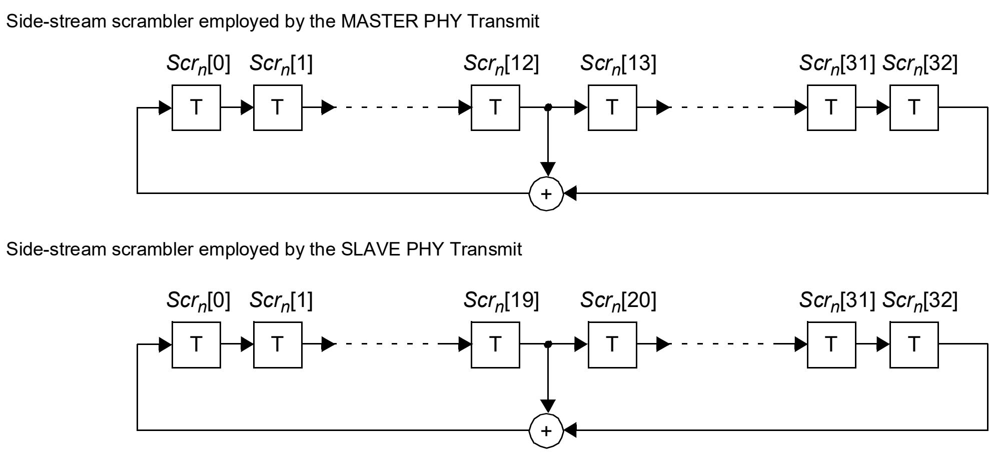


Figure 146–8—A realization of side-stream scramblers by linear feedback shift registers

146.3.3.4.2 Generation of $Sy_n[3:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the five bits $Sy_n[4:0]$. The four bits $Sy_n[3:0]$ are used for de-correlating the MII data word TXD<3:0> during data transmission and for generating the idle symbols. The bit $Sy_n[4]$ is used to randomize the frame delimiters. These five bits are generated as described below, using the auxiliary generating polynomial, g(x) defined in Equation (146–3):

$$g(x) = x^3 \wedge x^8 \quad (146\text{–}3)$$

The five bits $Sy_n[4:0]$ shall be generated using the bit $Scr_n[0]$ and $g(x)$ as in the following equations:

$$Sy_n[0] = Scr_n[0]$$
$$Sy_n[1] = g(Scr_n[0]) = Scr_n[3] \wedge Scr_n[8]$$
$$Sy_n[2] = g^2(Scr_n[0]) = Scr_n[6] \wedge Scr_n[16]$$
$$Sy_n[3] = g^3(Scr_n[0]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24].$$
$$Sy_n[4] = g^4(Scr_n[0]) = Scr_n[12] \wedge Scr_n[32]$$

By construction, the five bits $Sy_n[4:0]$ are derived from elements of the same maximum-length shift register sequence of length $2^{33}–1$ as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different so that there is no apparent correlation among the bits.

146.3.3.4.3 Generation of scrambled bits $Sd_n[3:0]$

From scrambler bits $Sy_n[3:0]$ and $TXD_n[3:0]$, bits $Sd_n[3:0]$ shall be generated as follows:

$$Sd_n[3] = \begin{cases} Sy_n[3] \wedge TXD_n[3] & \text{if (tx\_enable\_mii = TRUE)} \\ Sy_n[3] \wedge 1 & \text{else if (loc\_rcvr\_status = OK)} \\ Sy_n[3] & \text{else} \end{cases}$$

$$Sd_n[2] = \begin{cases} Sy_n[2] \wedge TXD_n[2] & \text{if (tx\_enable\_mii = TRUE)} \\ Sy_n[1] \wedge 1 & \text{else if (loc\_lpi = TRUE)} \\ Sy_n[1] & \text{else} \end{cases}$$

$$Sd_n[1:0] = \begin{cases} Sy_n[1:0] \wedge TXD_n[1:0] & \text{if (tx\_enable\_mii = TRUE)} \\ (Sy_n[2], Sy_n[0]) & \text{else} \end{cases}$$

Note that during transmission of idles, bits $Sy_n[1]$ and $Sy_n[2]$ shall be swapped, compared to data transmission, to reliably distinguish idle data transmission from data transmission at the receiver side.

146.3.3.5 Generation of code-groups

The PCS transmit state diagram generates code-groups as follows. A code-group $\{TA_n, TB_n, TC_n\}$ is sent in the following order: TA_n, TB_n, TC_n, TA_{n+1}, TB_{n+1}, TC_{n+1}, ...

146.3.3.5.1 Generation of code-groups in mode SEND_N and SEND_I

Both SEND_I and SEND_N use the following ternary symbol encoding. The scrambled bits $Sd_n[3:0]$ are converted to a code-group $\{TA_n, TB_n, TC_n\}$ using the 4B3T algorithm in conjunction with a running disparity value, shown in Table 146–1. The 4B3T coding is DC-free. To achieve this, the difference between the number of transmitted “+1” and “–1” symbols is limited. The running disparity reflects this difference and is used to choose the coding of the next symbol.

The code-group {0, 0, 0} is used as the COMMA value and never occurs during normal 4B3T mapping. This can also be used to synchronize the receiver’s demultiplexer code-group boundary during training.

Table 146–1—4B3T encoding

$Sd_n[3:0]$	Disparity = 1 $\{TA_n, TB_n, TC_n\}$		Disparity = 2 $\{TA_n, TB_n, TC_n\}$		Disparity = 3 $\{TA_n, TB_n, TC_n\}$		Disparity = 4 $\{TA_n, TB_n, TC_n\}$	
	Code-Group[1]	Disparity Change	Code-Group	Disparity Change	Code-Group	Disparity Change	Code-Group	Disparity Change
0000	+ 0 +	2	0 – 0	–1	0 – 0	–1	0 – 0	–1
0001	0 – +	0	0 – +	0	0 – +	0	0 – +	0
0010	+ – 0	0	+ – 0	0	+ – 0	0	+ – 0	0
0011	0 0 +	1	0 0 +	1	0 0 +	1	– – 0	–2
0100	– + 0	0	– + 0	0	– + 0	0	– + 0	0
0101	0 + +	2	– 0 0	–1	– 0 0	–1	– 0 0	–1
0110	– + +	1	– + +	1	– – +	–1	– – +	–1
0111	– 0 +	0	– 0 +	0	– 0 +	0	– 0 +	0
1000	+ 0 0	1	+ 0 0	1	+ 0 0	1	0 – –	–2
1001	+ – +	1	+ – +	1	+ – +	1	– – –	–3
1010	+ + –	1	+ + –	1	+ – –	–1	+ – –	–1
1011	+ 0 –	0	+ 0 –	0	+ 0 –	0	+ 0 –	0
1100	+ + +	3	– + –	–1	– + –	–1	– + –	–1
1101	0 + 0	1	0 + 0	1	0 + 0	1	– 0 –	–2
1110	0 + –	0	0 + –	0	0 + –	0	0 + –	0
1111	+ + 0	2	0 0 –	–1	0 0 –	–1	0 0 –	–1
NOTE–The Code-Group is {TAn, TBn, TCn}.								

[1]In Table 146–1 '–' is an abbreviation for the ternary symbol value '–1' and '+' is an abbreviation for the ternary symbol value '+1'.

The DISPRESET3 code-group, together with the following fourth code-group, is used to bring back the running disparity to a defined value of either 2 or 3, depending on the value of bit $Sy_n[4]$ from the scrambler. The coding shown in Table 146–2 is used for the DISPRESET3 code-group.

Table 146–2—Disparity reset

DISPRESET3	Disparity = 1	Disparity = 2	Disparity = 3	Disparity = 4
$Sy_n[4] = 0$	{–1, 0, +1}	{–1, 0, 0}	{–1, 0, –1}	{–1, –1, –1}
$Sy_n[4] = 1$	{+1, +1, +1}	{+1, 0, +1}	{+1, 0, 0}	{+1, 0, –1}

The fourth code-group (SSD4/ESD4/ESD_ERR4) is encoded as shown in Table 146–3:

Table 146–3—Delimiters

	Delimiter	$\{TA_n, TB_n, TC_n\}$
$Sy_n[4] = 0$	SSD4	{+1, +1, –1}
	ESD4	{+1, –1, +1}
	ESD_ERR4	{–1, +1, +1}
$Sy_n[4] = 1$	SSD4	{–1, –1, +1}
	ESD4	{–1, +1, –1}
	ESD_ERR4	{+1, –1, –1}

146.3.3.5.2 Generation of code-groups in mode SEND_Z

The code-group $\{TA_n, TB_n, TC_n\}$ is a zero vector {0, 0, 0} when tx_mode = SEND_Z.

146.3.4 PCS Receive

146.3.4.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 146–9 and associated state variables.

The received code-group Rx_n, generated by PCS Receive at time n, is decoded using the inverse of the mapping shown in Table 146–1. The result of the decoding is $Sr_n[3:0]$.

The PCS Receive function shall conform to the Receive watchdog state diagram in Figure 146–11. This prevents the possible lock-up of the PCS Receive state diagram in the DATA state due to mis-detection of an ESD. The maximum dwelling time in DATA state shall be less than the period specified for rcv_max_timer. When rcv_max_timer expires, the PCS Receive state diagram is reset and transitions to IDLE.

In Figure 146–9, there are a total of five states after SSD4 detection before the DATA state; meanwhile, there are also five states before the IDLE state (including the DATA state) that perform data decoding. As a result, the depth of the data flush-in delay line is the same as the flush-out delay line ensuring correct packet reception at the MII. These delay lines are necessary to decode the stream delimiters prior to forwarding the received data to the MII interface.

The variables, functions, and timers used in Figure 146–9, Figure 146–10, and Figure 146–11 (in 146.3.4.1.5) are defined next. For the definition of IDLE, COMMA, DISPRESET3, SSD4, ESD4, and ESD_ERR4, see 146.3.3.5.1.

146.3.4.1.1 Variables

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

receiving
: Generated by the PCS Receive function; if set as TRUE, it indicates that the PCS is in Data mode.
Values: TRUE or FALSE

loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

lpi_enabled
: This variable indicates whether Energy Efficient Ethernet is enabled for the PHY or not. If Auto-Negotiation is enabled, lpi_enabled reflects whether both PHYs have EEE capability advertised. If Auto-Negotiation is not enabled, and MDIO is implemented, lpi_enabled reflects bit 1.2294.10 as described in 45.2.1.186a.5.
Values: TRUE or FALSE

RX_ER
: The RX_ER signal of the MII as specified in 22.2.2.10.

RX_DV
: The RX_DV signal of the MII as specified in 22.2.2.7.

RXD[3:0]
: The RXD signal of the MII as specified in 22.2.2.8.

Rx_n
: Received code-group generated by PCS Receive at time n.

rx_lpi_active
: This variable indicates to the PMA receive function if the receive state diagram is in low power idle state.
Values: TRUE or FALSE

rx_symb_vector
: A vector of ternary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: single ternary symbol

rx_disparity
: PCS local variable containing the calculated running disparity at the receiver side. After PCS Reset, the initial value shall be set to 2.
Values: 1 to 4, depending on running disparity.

scr_status
: The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

disparity_error
: The disparity_error is set by the 4B3T decoder in the receiver, when a rx_code_group is received that is not allowed according to the running disparity calculated in the decoder.
Values: TRUE or FALSE

rcv_overrun_detected
: Variable set as TRUE when in RECEIVE OVERRUN state as shown in Receive watchdog state diagram in Figure 146–11 and set FALSE otherwise.
Values: TRUE or FALSE

146.3.4.1.2 Functions

valid_idle
: This function checks whether the decoded data bits $Sr_n[1:0]$ are equal to the expected $Sd_n[1:0]$ values from the local descrambler.
Values: TRUE or FALSE

check_idle
: The check_idle function indicates a reliable detection of the idle data stream.
Values: TRUE or FALSE

rem_lpi
: The rem_lpi function provides reliable detection of the received loc_lpi information from the remote PHY within the IDLE data stream.
Values: TRUE or FALSE

valid_dispreset
: Determines if the received code-group is one of the DISPRESET3 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the eight possible DISPRESET3 code-groups has been received.
Values: TRUE or FALSE

valid_ssd4
: Determines if the received code-group is one of the SSD4 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the two possible SSD4 code-groups has been received.
Values: TRUE or FALSE

valid_esd4
: Determines if the received code-group is one of the ESD4 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the two possible ESD4 code-groups has been received.
Values: TRUE or FALSE

valid_esd_err4
: Determines if the received code-group is one of the ESD_ERR4 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the two possible ESD_ERR4 code-groups has been received.
Values: TRUE or FALSE

DESCRAMBLE
: This function takes as its arguments the value of Rx_n and returns the descrambler output according to 146.3.4.3.

DECODE
: In the PCS Receive process, this function takes as its arguments the value of the received code-group and rx_disparity and returns the corresponding RXD[3:0] as well as the updated rx_disparity. DECODE follows the rules outlined in 146.3.4.2 and the inverse encoding rules stated in Table 146–1.

$RXD[3{:}0] = DESCRAMBLE(inverse\_table_{4B3T}(Rx_n))$

$rx\_disparity = rx\_disparity + disparity\ of\ currently\ received\ Rx_n$

CHECK_DISP
The CHECK_DISP function checks if the currently received code-group is allowed for the current rx_disparity, and returns TRUE or FALSE according to the relation:

$Rx_n \neq table_{4B3T}(inverse\_table_{4B3T}(Rx_n), rx\_disparity).$

The encoding rules for the 4B3T encoding are stated in Table 146–1.

RESET_DISP
This function takes as its argument the value of Rx_n, corresponding to a valid SSD4 code-group, and returns the updated rx_disparity as follows:

$$rx\_disparity = \begin{cases} 2, \text{ if } Rx_n = \{+1, +1, -1\} \\ 3, \text{ otherwise} \end{cases}$$

146.3.4.1.3 Timers

RSTCD
Abbreviation for Receive Symbol Tripled Conversion Done, which is equivalent to the timer condition rcv_symb_triplet_timer_done.

rcv_max_timer
A timer used to determine the maximum amount of time the Receive watchdog state diagram stays in the RECEIVE state. The timer shall expire 4 ms ± 100 µs after being started. The condition rcv_max_timer_done becomes true upon timer expiration.

rcv_symb_triplet_timer
The rcv_symb_triplet_timer is a continuous free-running timer that shall expire with three times the period of the receive symbol clock synchronously to PMA_UNITDATA.indication. RX_CLK (see 22.2.2.1) shall be generated from rcv_symb_triplet_timer with the falling edge of RX_CLK generated synchronously with rcv_symb_triplet_timer_done. During initial link training, the phase of the rcv_symb_triplet_timer is aligned to the receive symbol clock as described in 146.3.4.2.

Continuous timer: The condition rcv_symb_triplet_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration.

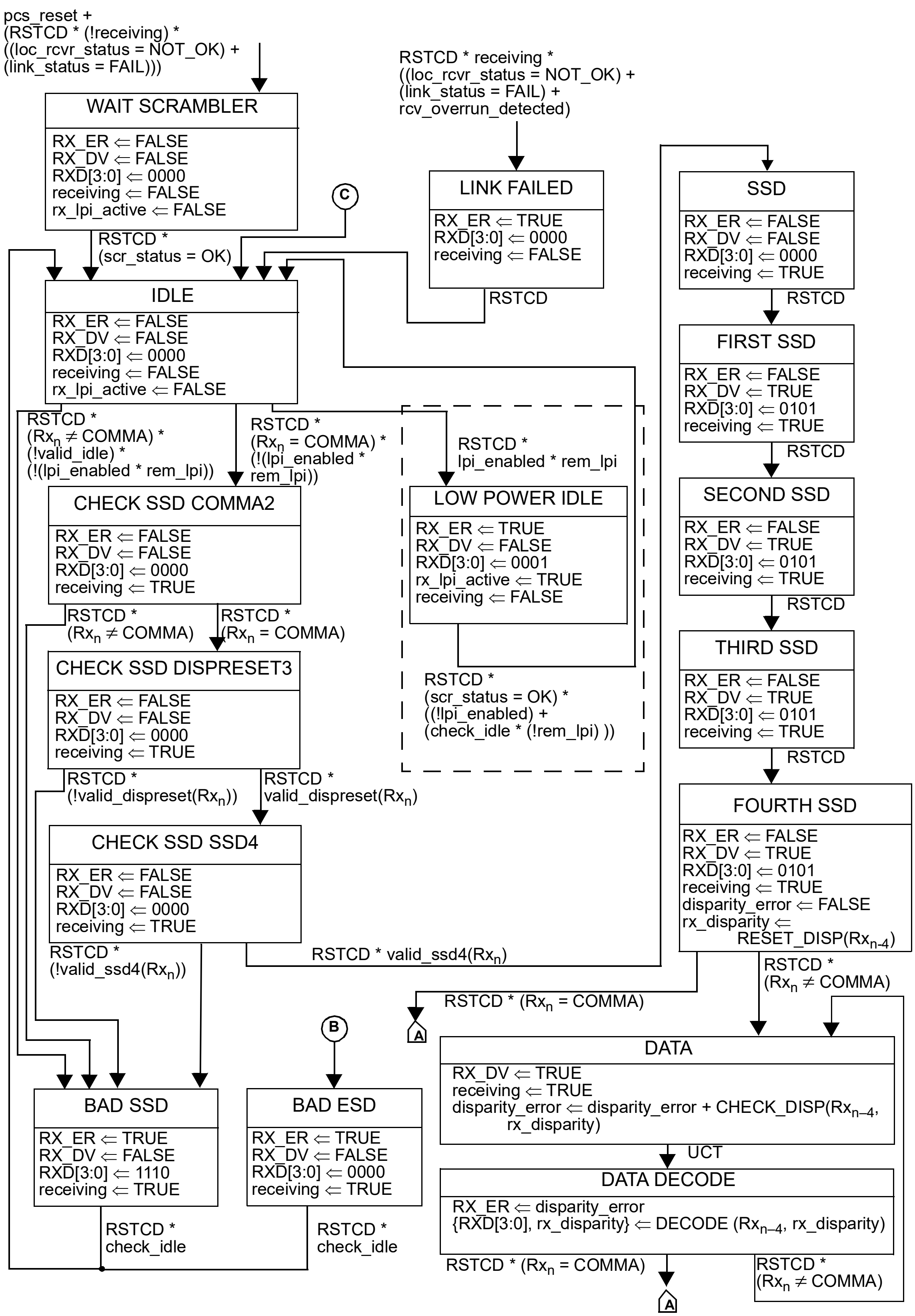
Duration: Three symbol times (see 146.5.4.5)

146.3.4.1.4 Constants

COMMA
A vector of three ternary symbols in the first or second code-group of any delimiter as specified in 146.3.3.5.1.

146.3.4.1.5 State diagrams

The PCS Receive state diagram is shown in Figure 146–9 and Figure 146–10 while the Receive watchdog state diagram is shown in Figure 146–11.



NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–9—PCS Receive state diagram, part a

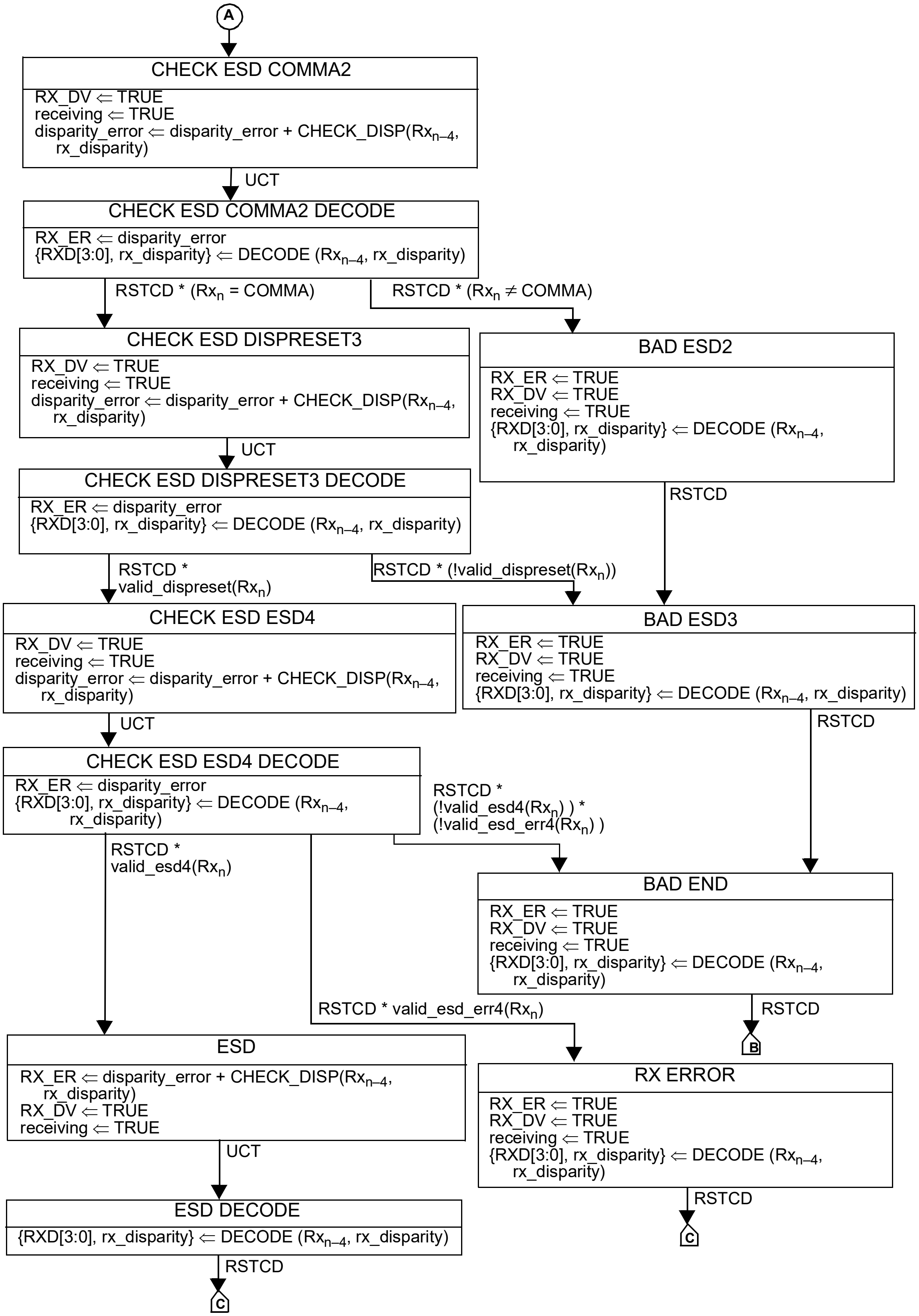


Figure 146–10—PCS Receive state diagram, part b

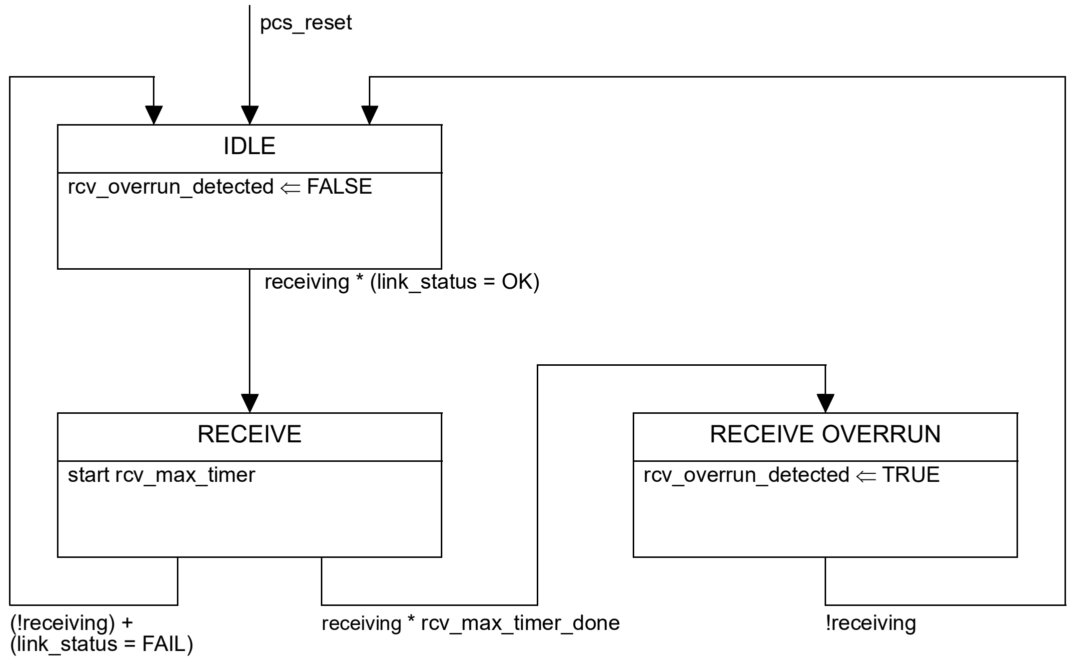


Figure 146–11—Receive watchdog state diagram

146.3.4.2 PCS Receive symbol decoding

When PMA Receive indicates normal operation and sets loc_rcvr_status = OK, the PCS Receive function checks the symbol sequences and searches for an SSD or a receive error indicator.

The received symbols, rx_symb_vector, are de-interleaved to generate received code-groups $\{RA_n, RB_n, RC_n\}$. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. The code-group {0, 0, 0} should never occur. The symbol synchronization in the de-interleaving block needs to be adjusted if the code-group {0, 0, 0} is being received. PCS Receive generates the sequence of symbols and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The descrambler can acquire synchronization during the PHY training.

The received code-groups $\{RA_n, RB_n, RC_n\}$ are decoded to generate signals RXD[3:0], RX_DV, and RX_ER at the MII. The decoder shall also generate the disparity_error signal for the PCS Receive state diagram when a code-group is received that is not allowed according to the current running disparity value. Each time a code-group is received, the running disparity is updated. This is done using the current running disparity and adding the disparity change value as specified in Table 146–1 for the currently received code-group.

PCS Receive shall set RX_DV = TRUE when it receives an SSD, and shall set RX_DV = FALSE when it receives an ESD or ESD with error.

PCS Receive shall set RX_ER = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs. When the state diagram reaches the IDLE state, RX_ER shall be reset to FALSE.

146.3.4.3 PCS Receive descrambler polynomial

The PHY decodes the code-groups and returns the proper bit stream to the descrambling process for generation of RXD<3:0> to the MII. For side-stream descrambling, the MASTER PHY shall employ the following receiver descrambler generator polynomial:

$$g'_M(x) = 1 + x^{20} + x^{33} \quad (146\text{–}4)$$

and the SLAVE PHY shall employ the following receiver descrambler generator polynomial:

$$g'_S(x) = 1 + x^{13} + x^{33} \quad (146\text{–}5)$$

146.3.4.4 PCS Receive automatic polarity detection

An automatic polarity detection and correction shall be implemented on the receive side of both master and slave PHY.

Polarity can be automatically detected in a recursive process: one assumption of polarity is made first and the descrambler synchronization is monitored within a certain period to determine whether such an assumption is correct; if not, the same procedure is repeated with a different polarity assumption and vice versa.

Receive polarity detection and correction can be done simultaneously at the earliest link up stages. Link up starts with the MASTER PHY sending symbols to the SLAVE PHY. If a polarity flip is detected, the SLAVE changes the sign of its received signals $\{RA_n, RB_n, RC_n\}$ to correct the polarity. There is no change in the polarity of the transmit signal. After the SLAVE PHY has started transmission, the MASTER PHY can use the same method for determining its receive polarity.

146.3.5 PCS loopback

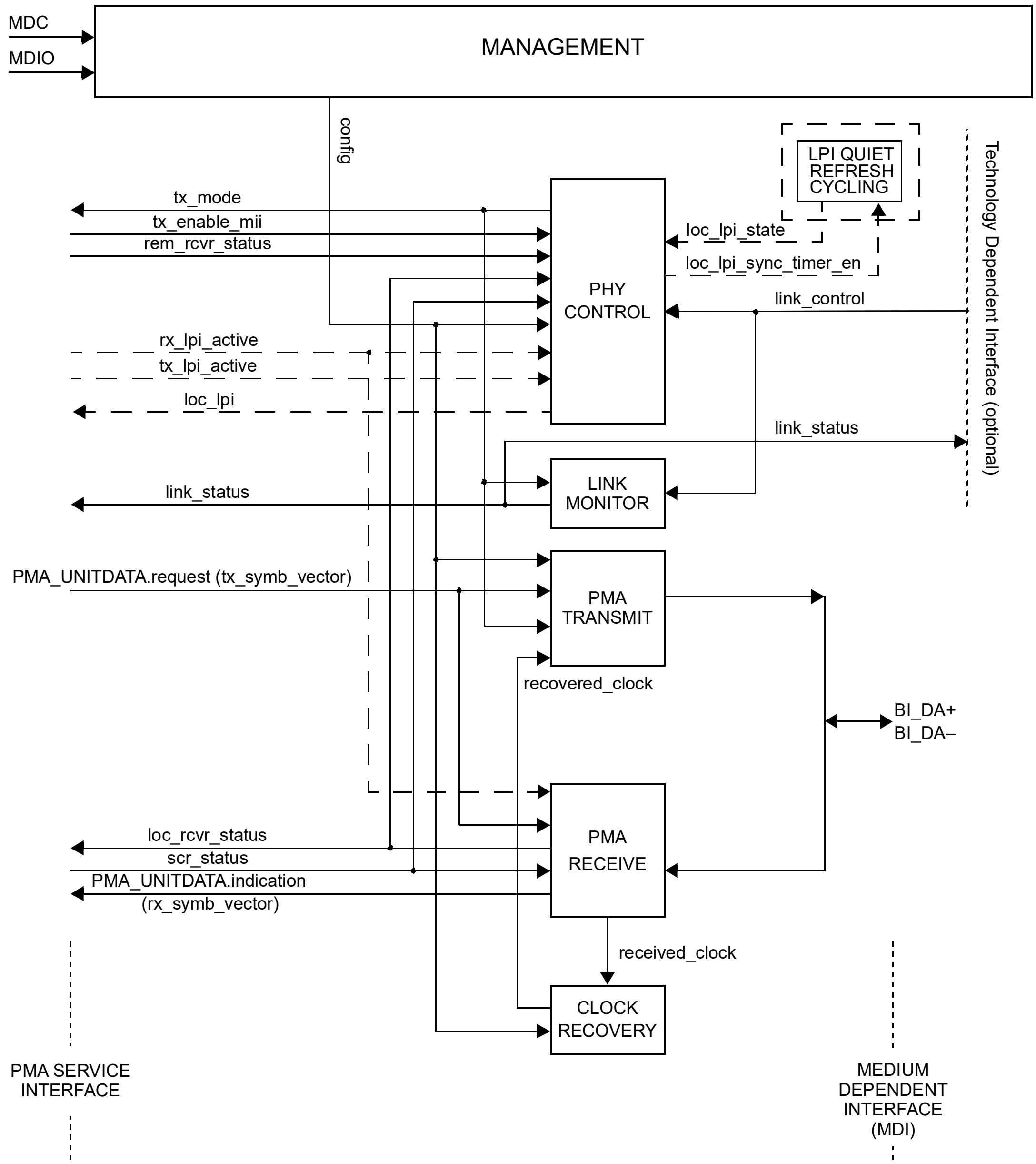
The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, or the loopback bit in MDIO register 3.2278.14, defined in 45.2.3.68a.2, is set to one (or by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.

NOTE—The signal path through the PCS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompasses as much of the PCS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function testing the transmit and receive data paths.

146.4 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PMA service interface specified in 146.3 onto the 10BASE-T1L physical medium, and provides the link management and PHY Control functions. The PMA provides full duplex communications to and from medium employing 3-level Pulse Amplitude Modulation (PAM3). The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 146.8.

PMA functions are illustrated in Figure 146–12.



NOTE 1—The "recovered_clock" shown indicates the delivery of the recovered clock back to PMA TRANSMIT in SLAVE mode for loop timing.

NOTE 2—Signals shown with dashed lines and blocks within dashed lines are required only for EEE functionality.

Figure 146–12—PMA functional block diagram

146.4.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PMA Reset shall set pma_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

146.4.2 PMA Transmit function

Figure 146–13 illustrates the signal flow of the 10BASE-T1L PMA Transmit function. During transmission, PMA_UNITDATA.request conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over the single transmit pair.

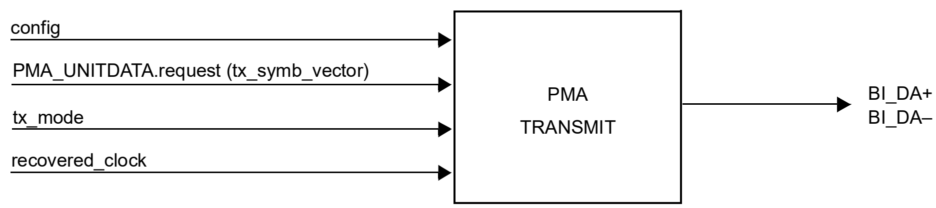


Figure 146–13—PMA Transmit

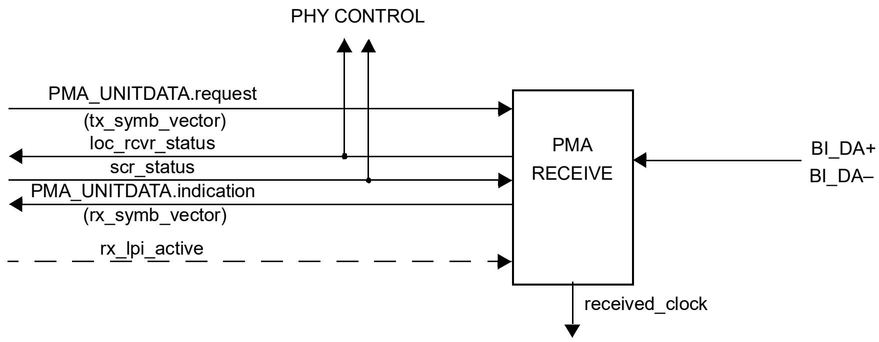
A single transmitter is used to generate the PAM3 signal BI_DA on the wire using the transmit clock, TX_TCLK (see 146.5.4.5). When the config parameter is set to MASTER, the PMA Transmit function derives the TX_TCLK from a local clock source. When the config parameter is set to SLAVE, the PMA Transmit function derives the TX_TCLK from the recovered clock.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

146.4.3 PMA Receive function

Figure 146–14 illustrates the signal flow of the 10BASE-T1L PMA Receive function. To achieve the indicated performance, it is highly recommended that PMA Receive includes the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb_vector is needed to perform echo cancellation.

The 10BASE-T1L PMA Receive function comprises a single receiver (PMA Receive) for PAM3 modulated signals on a single balanced pair, BI_DA. PMA Receive has the ability to translate the received signals on the MDI into the PMA_UNITDATA.indication parameter rx_symb_vector. It detects ternary symbol sequences from the signals received at the MDI and presents these sequences to the PCS Receive function. The parameter loc_rcvr_status is generated by PMA Receive to indicate the status of the receive link at the local PHY. This variable indicates to the PCS Transmitter, PCS Receiver, and PMA PHY Control function whether the status of the overall received link is ok or not. Signal scr_status is generated by the PCS Receiver to indicate the status of the descrambler to the local PHY. It conveys the information on whether the scrambler has achieved synchronization or not to the PMA receive function.



NOTE—Signals shown with dashed lines are required only for EEE functionality.

Figure 146–14—PMA Receive

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.186b.7.

146.4.4 PHY Control function

If the Auto-Negotiation process (Clause 98) is not implemented or not enabled, PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

The PHY Control functions block governs the control actions needed to bring the PHY into the 10BASE-T1L mode of operation so that frames can be exchanged with the link partner. PMA PHY Control also generates the signals that control PCS and PMA sublayer operations. It determines whether the PHY operates in the normal mode, enabling data transmission over the link segment, or whether the PHY sends idle data. PHY Control sets tx_mode to SEND_N (transmission of normal MII Data Stream, Control Information, or Idle Data), SEND_I (transmission of Idle Data), or SEND_Z (transmission of zero symbol vectors).

If the time to reach link_status = OK exceeds the duration of the link_fail_inhibit timer used in the Auto-Negotiation Arbitration state diagram (see Figure 98–7), the training may be considered failed. Management reset of the PHY control state diagram when Auto-Negotiation is not enabled (or not present) is outside the scope of this standard.

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs shall synchronize refresh intervals during the low power idle (LPI) mode.

LPI synchronization is established by the PHY Control function, towards the end of link startup, using a handshake scheme initiated by the MASTER. This scheme initiates LPI quiet-refresh cycling at the same time as a transition from TRUE to FALSE of the loc_lpi variable. As loc_lpi is conveyed to the link partner PHY, the time of the start of LPI quiet-refresh cycling is also conveyed. LPI quiet-refresh cycling is defined in 146.4.7.

Thereafter, the LPI quiet-refresh cycling runs freely, with a cycle of fixed period, and, because the SLAVE maintains timing lock with the MASTER, the timing relationship between the quiet-refresh cycling in both PHYs remains fixed.

PHY Control shall comply with the state diagram shown in Figure 146–15, Figure 146–16, and Figure 146–17. Figure 146–15 describes link startup sequencing. Figure 146–16 describes LPI synchronization sequencing (required only to support EEE capability). Figure 146–17 describes entry and exit to LPI mode (also required only to support EEE capability).

146.4.4.1 Variables

pma_reset
: Allows reset of all PMA functions.
Values: TRUE or FALSE
Set by: PMA Reset

link_control
: This variable is set by management control or via hardware.
Values: ENABLE or DISABLE

config
: The config parameter is set by management or set by auto-negotiation and passed to the PMA and PCS.
Values: MASTER or SLAVE

loc_lpi:
: The variable loc_lpi is set by the PHY Control function to indicate that it has entered low power idle mode.
Values: TRUE or FALSE

loc_lpi_timer_sync_en
: The variable loc_lpi_timer_sync_en is set by the PHY Control function to enable low power idle quiet-refresh cycling.
Values: TRUE: LPI quiet-refresh cycling is enabled.
FALSE: LPI quiet-refresh cycling is disabled.

loc_rcvr_status
: Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive function for the local PHY.
Values: OK: The receive function for the local PHY is operating reliably.
NOT_OK: Operation of the receive function for the local PHY is unreliable.

lpi_enabled
: This variable indicates whether Energy Efficient Ethernet is enabled for the PHY or not.
Values: TRUE: Energy Efficient Ethernet is enabled.
FALSE: Energy Efficient Ethernet is not enabled.

mr_autoneg_enable
: See 98.5.1.

rem_rcvr_status
: Variable set by the PCS Receive function to indicate whether correct operation of the receive function for the remote PHY is detected or not.
Values: OK: The receive function for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive function for the remote PHY is not detected.

rx_lpi_active
: This variable indicates to the PMA receive function if the receive state diagram is in low power idle state.
Values: TRUE or FALSE

scr_status

The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

slave_clock_locked

Variable indicates the status of the clock recovery on a slave PHY. Implementations may benefit from checking scr_status for determining whether the slave clock is locked to the master PHY.
Values: TRUE: The slave clock is stable and locked to the master PHY clock.
FALSE: The slave clock is not locked to the master PHY clock, or is otherwise unstable.

tx_enable_mii

The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4. When set to FALSE transmission is disabled; when set to TRUE transmission is enabled.
Values: TRUE or FALSE

tx_lpi_active

This variable indicates to the PMA PHY control function whether the "Assert Low Power Idle" condition on the MII is active.
Values: TRUE or FALSE

tx_mode

PCS Transmit sends code-groups according to the value of this variable.
Values: SEND_N: This value is continuously asserted when transmitting data, control information or idle during normal operation.
SEND_I: This value is continuously asserted when transmitting idle data during training.
SEND_Z: This value is asserted when transmitting zero code-groups.

146.4.4.2 Timers

maxtraining_timer

A timer used to limit the maximum allowed training time of the receiver. The timer shall expire 3000 ms ± 30 ms after being started.

mintraining_timer

A timer to define the minimum time a slave PHY stays in training mode before going to SILENT state when the slave loses clock lock. The slave clock may be unstable during this period. The timer shall expire 100 ms ± 1 ms after being started.

lpi_sleep_timer

A timer used to determine the duration of the SEND SLEEP state, where transmission comprises IDLE symbols with loc_lpi set. The timer shall expire 150 TX_TCLK periods (nominally 20 μs) after being started.

lpi_wake_timer

A timer used to determine how long the WAKE signal is being sent to the remote PHY. The timer shall expire 1875 TX_TCLK periods (nominally 250 μs) after being started.

maxwait_timer

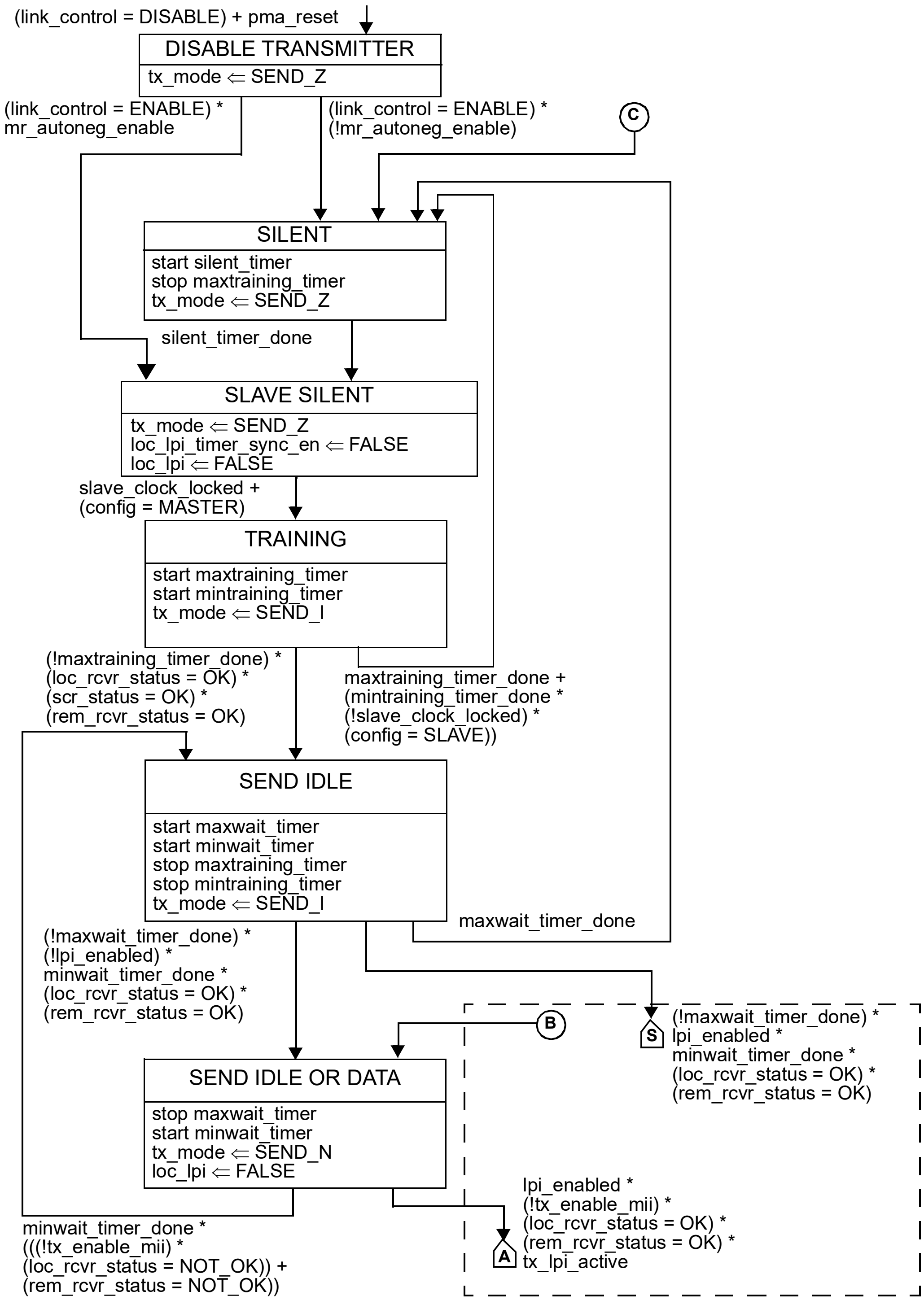
A timer used to limit the amount of time during which a receiver dwells in the SEND IDLE state. The timer shall expire 200 ms ± 2 ms after being started.

minwait_timer
: A timer used to determine the minimum amount of time the PHY Control stays in the SEND IDLE or DATA states. The timer shall expire 20 μs ± 1 μs after being started.

silent_timer
: A timer used to set the time a PHY stays in the SILENT state. The timer shall expire 245 ms ± 5 ms after being started.

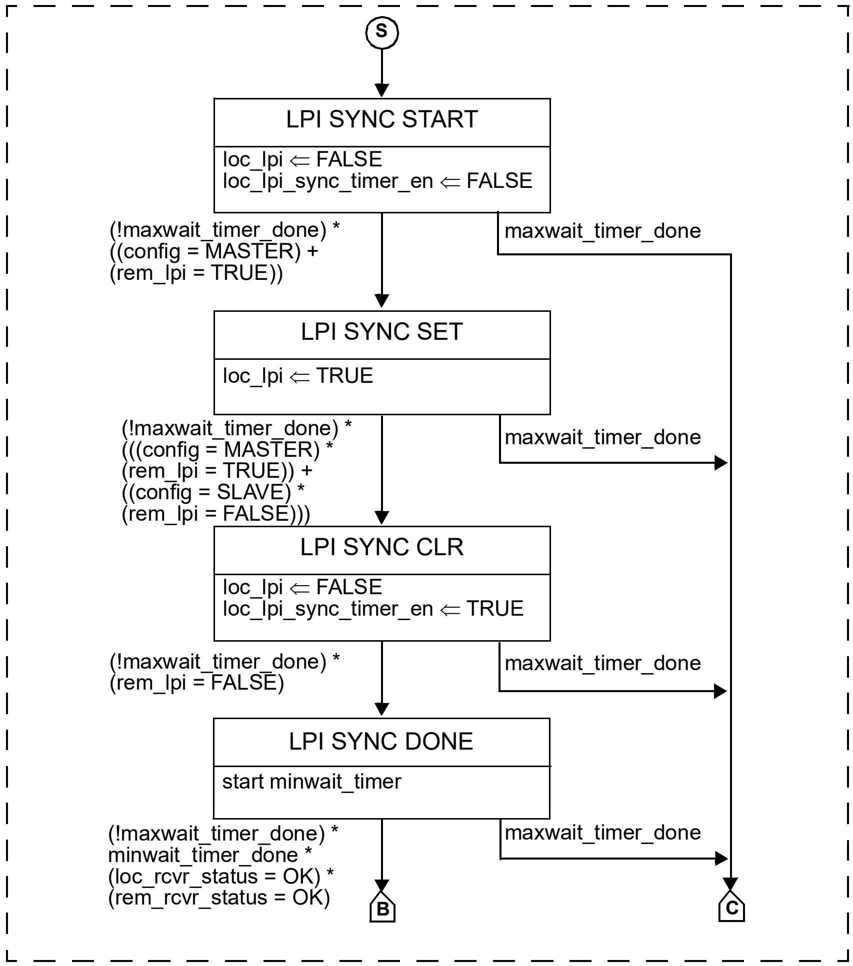
NOTE—After a disturbance on the link segment, e.g., when the current consumption on a powered link segment is quickly changed, the maxwait_timer allows the PHYs to stay in the SEND IDLE state before going to the SILENT state. This allows the PHYs to attempt to recover the link before a full retrain.

146.4.4.3 State diagram



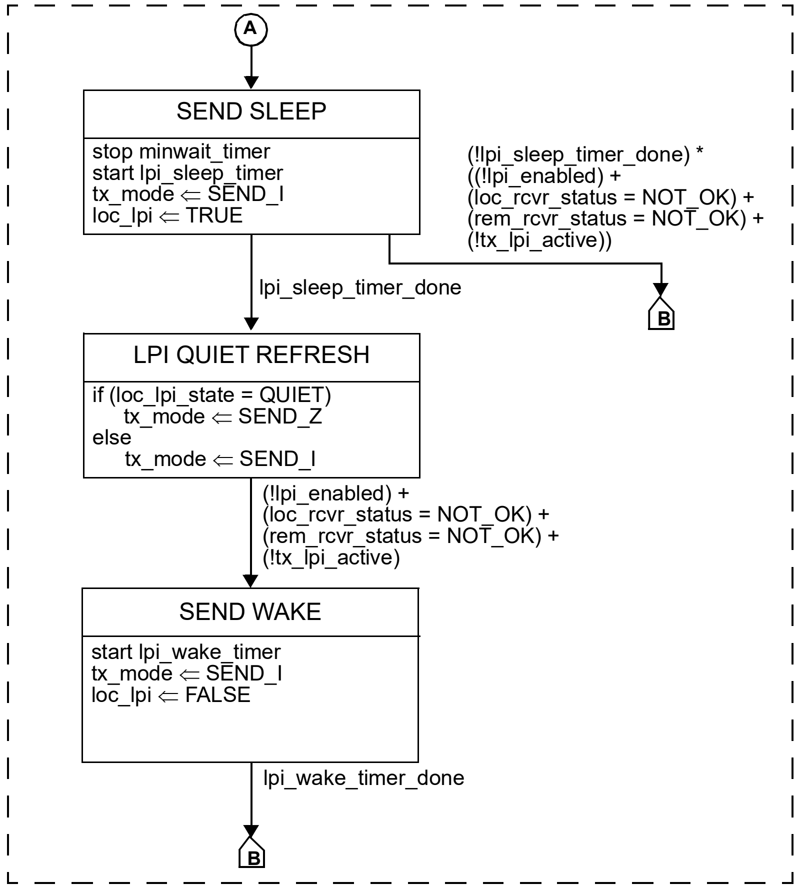
NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–15—PHY Control state diagram, part a



NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–16—PHY Control state diagram, part b



NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–17—PHY Control state diagram, part c

146.4.5 Link Monitor function

Link Monitor operation, as shown in state diagram of Figure 146–18, shall be provided to support PHY Control. Variable link_control is set to ENABLE through management control during the PHY initialization or via default hardware set-up.

146.4.5.1 Variables

tx_mode

The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

146.4.5.2 State diagram

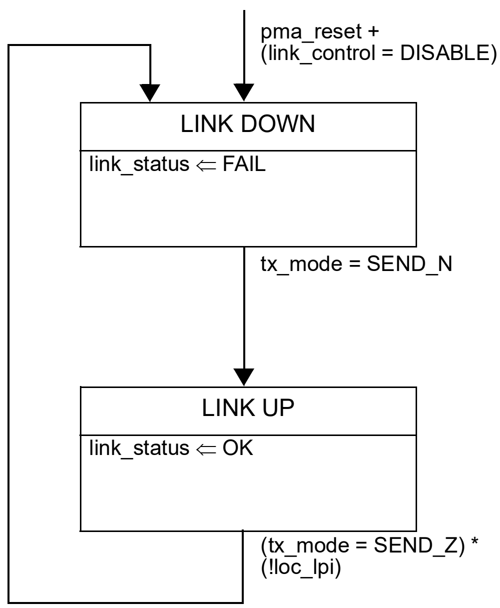


Figure 146–18—PHY Link Monitor state diagram

146.4.6 PMA clock recovery

The clock recovery provides a synchronous clock for sampling the signal on the pair. While it may not drive the MII directly, the Clock Recovery function is the underlying source of TX_CLK. This PMA function recovers the clock from the received stream. It is coupled to the receiver in order to provide for the SLAVE PHY a clock synchronous to the transmit clock of the MASTER PHY.

146.4.7 LPI quiet-refresh cycling

LPI quiet-refresh cycling is initiated on direction from the PHY Control function using the LPI synchronization mechanism.

Once initiated, LPI quiet-refresh cycling runs freely for the lifetime of the link.

The SLAVE PHY is required to implement an initial offset delay, to ensure that refresh intervals of MASTER and SLAVE are not coincident.

The quiet-refresh cycle timing is defined in terms of transmit symbol periods (TX_TCLK periods). As the SLAVE must maintain timing lock with the MASTER, the timing relationship between the LPI quiet-refresh cycling of the two PHYs must remain fixed for the lifetime of the link.

LPI quiet-refresh cycling shall comply with the state diagram of Figure 146–19.

146.4.7.1 Variables

loc_lpi_timer_sync_en
: The variable loc_lpi_timer_sync_en is set by the PHY Control function to enable low power idle quiet-refresh cycling.
: Values: TRUE: LPI quiet-refresh cycling is enabled.
: FALSE: LPI quiet-refresh cycling is disabled.

loc_lpi_state
: The variable loc_lpi_state sets the quiet-refresh state when the PHY is in low power idle mode.
: Values: IDLE: LPI quiet-refresh cycling is not enabled.
: REFRESH: The PHY is in the low power idle refresh phase.
: QUIET: The PHY is in the low power idle quiet phase.

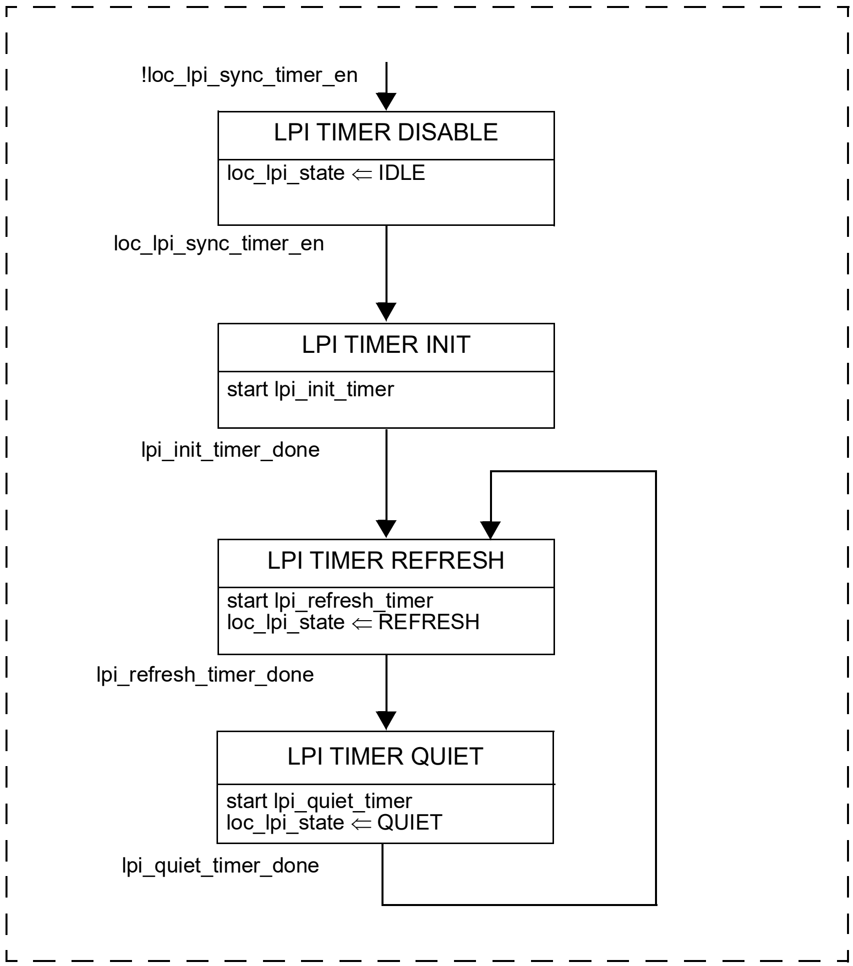
146.4.7.2 Timers

lpi_init_timer
: A timer used to set the duration of the LPI TIMER INIT state, which is intended to introduce a fixed offset between LPI refresh phases of the MASTER and SLAVE PHYs.
: If config = MASTER, this timer shall expire after 0 TX_TCLK periods.
: If config = SLAVE, this timer shall expire after 22500 TX_TCLK periods (nominally 3000 μs).

lpi_refresh_timer
: A timer used to set the duration of the LPI refresh phase.
: This timer shall expire after 1875 TX_TCLK periods (nominally 250 μs).

lpi_quiet_timer
: A timer used to set the duration of the LPI quiet phase.
: This timer shall expire after 45 000 TX_TCLK periods (nominally 6000 μs).

146.4.7.3 State diagram



NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–19—LPI quiet-refresh cycling state diagram

146.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1L Ethernet PHY.

146.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 146.5.1.1 and 146.5.1.2 can be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements.

146.5.1.1 Immunity—DPI test

In a real application, radio frequency (RF) common mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise can be tested according to the DPI method of IEC 62132-4.

146.5.1.2 Emission—Conducted emission test

The emission of the PMA transmitter to its electrical environment can be tested according to the 150 Ω direct coupling method of IEC 61967-4.

146.5.2 Test modes

The test modes described in this subclause are provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. Test modes 1 through 3 shall be implemented as follows. The test modes can be enabled by setting bits 1.2296.15:13 (10BASE-T1L Test Mode Control Register) of the PHY Management register set as described in 45.2.1.186c.1. If MDIO is not implemented, a similar functionality shall be provided by another interface. These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1—Transmitter output voltage and timing jitter test mode
b) Test mode 2—Transmitter output droop test mode
c) Test mode 3—Normal operation in Idle mode. This is for the PSD mask test.

When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, –1). See 146.5.4.5 for transmit clock requirements.

When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "–1" symbols. This sequence is repeated continually.

When test mode 3 is enabled, the 10BASE-T1L PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals.

146.5.3 Test fixture

The following fixtures (illustrated by Figure 146–20 and Figure 146–21), or their functional equivalents, can be used for measuring the transmitter specifications described in 146.5.4. All the transmitter tests are defined at the MDI.

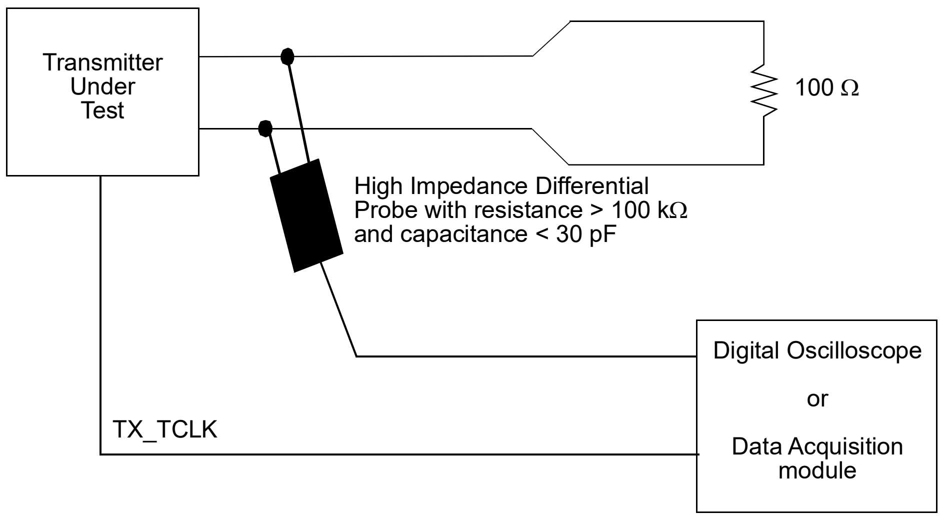


Figure 146–20—Transmitter test fixture 1 for transmitter voltage, transmitter droop, and transmitter timing jitter

To allow an easy synchronization of the measurement equipment, the PHY shall provide access to the symbol rate clock TX_TCLK, which times the transmitted symbols. For a MASTER PHY this is the output of the (divided) clock oscillator; for the SLAVE PHY this is the recovered clock.

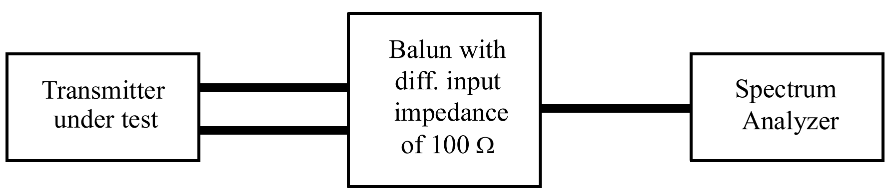


Figure 146–21—Transmitter test fixture 2 for power spectral density measurement and transmit power level measurement

146.5.4 Transmitter electrical specifications

The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of 146.5.4 with a 100 Ω ± 0.1% resistive differential load connected to the transmitter output.

146.5.4.1 Transmitter output voltage

When tested with the test fixture shown in Figure 146–20 with the transmitter in test mode 1, the transmitter output voltage shall be 2.4 V + 5%/– 15% peak-to-peak (for the 2.4 Vpp operating mode) and 1.0 V + 5%/– 15% peak-to-peak (for the 1.0 Vpp operating mode). Transmitter output voltage can be set using the management interface or by hardware default set-up.

NOTE—In all transmit modes, including SEND_I and SEND_N, when measured with a 100 Ω ± 0.1% termination, the transmit differential signal at the MDI is less than 2.64 Vpp for the 2.4 Vpp operating mode and 1.10 Vpp for the 1.0 Vpp operating mode including the signal droop.

146.5.4.2 Transmitter output droop

With the transmitter in test mode 2 and using the transmitter test fixture shown in Figure 146–20, the magnitude of both the positive and negative droop shall be less than 10% measured with respect to an initial value at 133.3 ns after the zero crossing and a final value at 800 ns after the zero crossing.

146.5.4.3 Transmitter timing jitter

When tested using the test fixture shown in Figure 146–20 with the transmitter in test mode 1, the maximum jitter at the transmitter side shall be less than 10 ns symbol-to-symbol jitter.

146.5.4.4 Transmitter Power Spectral Density (PSD) and power level

In test mode 3 (reflecting normal operation), the transmit power shall be 8.6 ± 1.2 dBm for the 2.4 Vpp operating mode and 1.0 ± 1.2 dBm for the 1.0 Vpp operating mode. The power spectral density of the transmitter, measured into a 100 Ω load using the test fixture shown in Figure 146–21, shall be between the upper and lower masks specified in Equation (146–6) and Equation (146–7) for the 2.4 Vpp transmit amplitude, and by Equation (146–8) and Equation (146–9) for the 1.0 Vpp transmit amplitude. The masks are shown in Figure 146–22 and Figure 146–23.

For the 2.4 Vpp transmit signal amplitude:

$$\text{Upper PSD Limit }(f) \geq \begin{cases} -54 \text{ dBm/Hz} & 0 \leq f \leq 2.5 \\ -54 - 1.6 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f < 12.5 \\ -70 \text{ dBm/Hz} & 12.5 \leq f \leq 20 \end{cases} \tag{146–6}$$

$$\text{Lower PSD Limit }(f) \geq \begin{cases} -60 \text{ dBm/Hz} & 0.625 \leq f \leq 2.5 \\ -60 - 4 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f \leq 5 \end{cases} \tag{146–7}$$

where f is the frequency in MHz, and for the 1.0 Vpp transmit signal amplitude:

$$\text{Upper PSD Limit }(f) \geq \begin{cases} -61.6 \text{ dBm/Hz} & 0 \leq f \leq 2.5 \\ -61.6 - 1.6 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f < 12.5 \\ -77.6 \text{ dBm/Hz} & 12.5 \leq f \leq 20 \end{cases} \tag{146–8}$$

$$\text{Lower PSD Limit }(f) \geq \begin{cases} -67.6 \text{ dBm/Hz} & 0.625 \leq f \leq 2.5 \\ -67.6 - 4 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f \leq 5 \end{cases} \tag{146–9}$$

where f is the frequency in MHz.

.

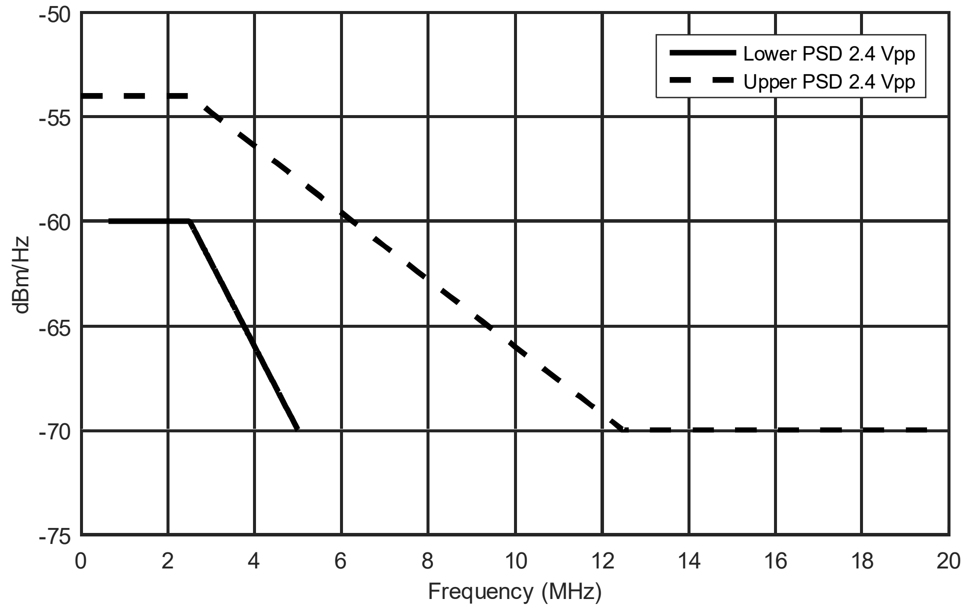


Figure 146–22—Transmitter Power Spectral Density, 2.4 Vpp Transmit Amplitude, Upper and Lower Masks

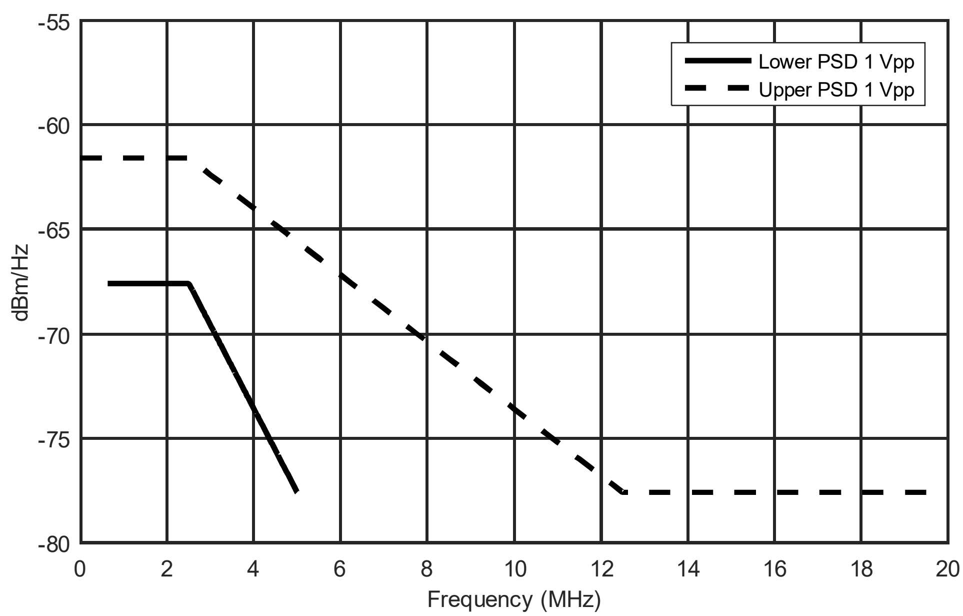


Figure 146–23—Transmitter Power Spectral Density, 1 Vpp Transmit Amplitude, Upper and Lower Masks

146.5.4.5 Transmit clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 7.5 MBd ± 50 ppm. For a MASTER PHY, when the transmitter is in the LPI transmit mode, the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

146.5.5 Receiver electrical specifications

The PMA shall meet the requirements specified in PMA Receive function and the electrical specifications of this subclause. The link segment used in the test configurations shall be within the limits specified in 146.7.

146.5.5.1 Receiver differential input signals

Differential signals received at the MDI, that were transmitted from a remote transmitter within the specifications of 146.5.4, and have passed through a link segment specified in 146.7, shall be received with a bit error ratio less than 10^{-9} after PCS processing and sent to the MII after completion of link training. This specification can be verified by a frame error ratio less than 10^{-6} for 125 octet frames.

146.5.5.2 Receiver frequency tolerance

The receiver shall properly receive incoming data with a symbol rate within the range 7.5 MBd ± 50 ppm.

146.5.5.3 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source such that noise with a Gaussian distribution, bandwidth of 10 MHz, and magnitude of –106 dBm/Hz is present at the MDI. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 146–24, with a link segment as defined in 146.7. The BER shall be less than 10^{-9}. This specification may be considered satisfied when the frame loss ratio is less than 10^{-6} for 125 octet packets measured at MAC/PLS service interface.

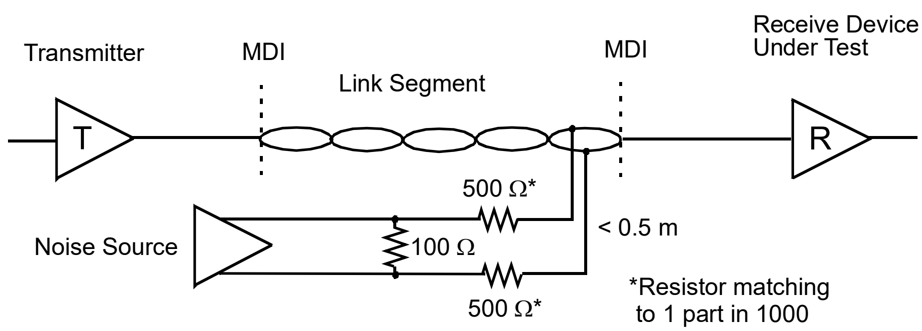


Figure 146–24—Alien crosstalk noise rejection test set-up

NOTE—If the output level is too high for the noise generator, the resistor divider network may be adapted to allow for a lower noise generator output level so that the noise signal fed into the receiver has a magnitude of –106 dBm/Hz with a bandwidth of 10 MHz, taking the 100 Ω termination within the PHY into account.

146.5.6 PMA local loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or the PMA loopback bit in MDIO register 1.2294.0, defined in 45.2.1.186a.6, is set to one (or PMA loopback mode is enabled by a similar functionality if MDIO is not implemented). When the PHY is in the PMA local loopback mode, the PMA Receive function utilizes the echo signals from the open MDI and decodes these signals to pass the data back to the MII Receive interface. The data flow of the external loopback is shown in Figure 146–25. When PMA loopback mode is present and enabled, the PCS transmit scrambler polynomial and the receiver descrambler polynomial should be matched, e.g., the MASTER scrambler polynomial and the SLAVE descrambler polynomial, in order for looped data to be properly descrambled at the MII.

A MAC client can compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 10BASE-T1L PCS and PMA functions.

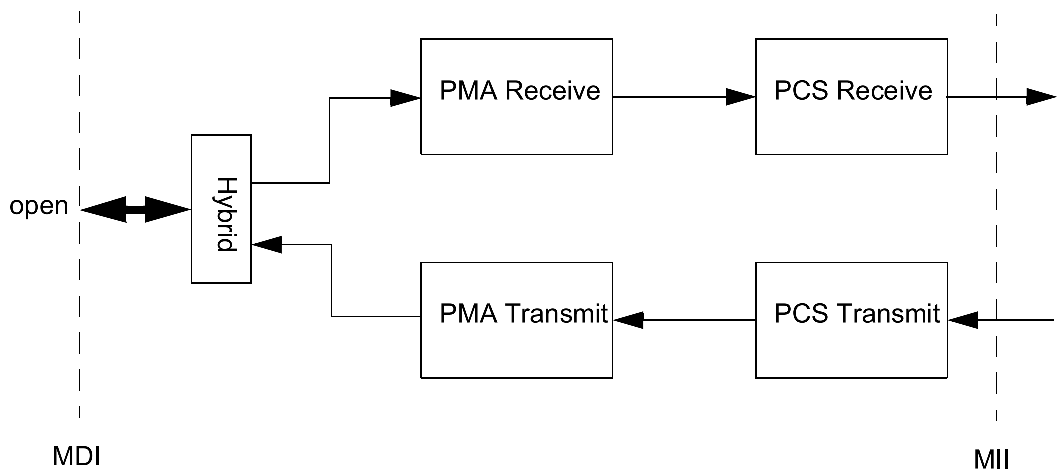


Figure 146–25—PMA loopback data flow

146.6 Management interface

10BASE-T1L uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

146.6.1 Support for Auto-Negotiation

If Auto-Negotiation is supported and enabled, the mechanism described in Clause 98 shall be used. Auto-Negotiation may be performed as part of the initial set-up of the link and allows negotiation of MASTER/SLAVE for loop timing, increased transmit level, and EEE capabilities.

146.6.2 MASTER-SLAVE configuration

MASTER-SLAVE assignment for each link configuration is necessary for establishing the timing control of each PHY. In 10BASE-T1L, one PHY should be configured as MASTER and one PHY should be configured as SLAVE to operate. In the case where both PHYs are configured to be MASTER or both to be SLAVE, operation is undefined.

If Auto-Negotiation is available and enabled, the MASTER-SLAVE configuration between the PHYs is established using the method being described in 98.2.1.2.5 and Table 98-4. If there is no Auto-Negotiation functionality present or if Auto-Negotiation function has been disabled, the MASTER-SLAVE configuration is performed for each PHY using bit 1.2100.14 (BASE-T1 PMA/PMD control register) or equivalent functionality.

146.6.3 PHY initialization

Both PHYs sharing a link segment are capable of being MASTER or SLAVE. A forced assignment scheme or an Auto-Negotiation process is employed depending on the use case of the PHY. This process is conducted at the power-up or reset condition. The station management systems can manually configure the 10BASE-T1L PHY to be MASTER or to be SLAVE (before the link acquisition process starts) or a hardware set-up using bootstrap options can be implemented.

When MDIO is implemented, MASTER/SLAVE mode can be selected by setting bit 1.2100.14 (BASE-T1 PMA/PMD Control Register) of the PHY Management register set as described in 45.2.1.185. If MDIO is not implemented, a similar functionality shall be provided by another interface. The default setting is to use Auto-Negotiation, if available.

146.6.4 Increased transmit level configuration

The transmitter output voltage can be selected by setting bit 1.2294.12 (10BASE-T1L PMA control register) of the PHY Management register set as described in 45.2.1.186a.3 if Auto-Negotiation is disabled or not present. If MDIO is not implemented, a similar functionality shall be provided by another interface.

When Auto-Negotiation is implemented and enabled, bit A23 shall contain a one if the PHY is requesting the increased transmit level from its link partner, and it shall contain a zero if the 2.4 Vpp operating mode is not requested from the link partner (see 146.5.4.1). Bit A24 shall contain a one if the PHY is supporting and advertising the 2.4 Vpp operating mode, and it shall contain a zero if the 2.4 Vpp operating mode is not supported or not advertised.

When Auto-Negotiation is present and enabled and both PHYs advertise an increased transmit/receive ability if at least one PHY requests the 10BASE-T1L increased transmit level, then both PHYs shall use the 2.4 Vpp operating mode, in all other cases both PHYs shall use the 1.0 Vpp operating mode.

146.6.5 EEE configuration

When Auto-Negotiation is implemented and enabled, bit A25 shall contain a one if the 10BASE-T1L PHY is supporting and advertising Energy Efficient Ethernet ability and it shall contain a zero if Energy Efficient Ethernet is not supported or not advertised.

146.6.6 PMA and PCS MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA and PCS. When MDIO is implemented, mapping of MDIO register bits to PMA and PCS control/status variables is shown in Table 146–4. If no MDIO is implemented, a similar functionality shall be implemented to access the needed variables.

Table 146–4—MDIO register bit mapping

Register Name	Register/Bit Number	Control/Status variable
BASE-T1 PMA/PMD control register	1.2100.3:0	T1 PHY type selection
BASE-T1 PMA/PMD control register	1.2100.14	Master/Slave mode
PMA/PMD Control 1 register 10BASE-T1L PMA control register	1.0.15 1.2294.15	pma_reset
PMA/PMD Control 1 register 10BASE-T1L PMA control register	1.0.0 1.2294.0	PMA loopback
PMA/PMD Status 1 register 10BASE-T1L PMA status register	1.1.2 1.2295.0	link_status
10BASE-T1L PMA control register	1.2294.12	Transmit voltage amplitude control
PCS Control 1 register 10BASE-T1L PCA control register	3.0.15 3.2278.15	pcs_reset
PCS Control 1 register 10BASE-T1L PCA control register	3.0.14 3.2278.14	PCS loopback

146.7 Link segment characteristics

10BASE-T1L is designed to operate over a single balanced pair of conductors that meets the requirements specified in this subclause. The single balanced pair of conductors supports an effective data rate of 10 Mb/s in each direction simultaneously. The term “link segment” used in this clause refers to a single balanced pair of conductors operating in full duplex. Note that Annex 146B provides information on the optional powering topologies. The class power requirements are specified in Clause 104.

The link segment specified in this clause is based on process control application requirements and supports up to ten in-line connectors using a single balanced pair of conductors for up to at least 1000 m.

146.7.1 Link transmission parameters for 10BASE-T1L

The transmission characteristics for the 10BASE-T1L link segment are specified to support applications requiring long reach such as industrial and process control, for up to at least 1000 m. 10BASE-T1L link segments may be shielded or screened, consistent with the specification in 146.7.1.6 and 146.7.2 or unshielded consistent with the specifications in 146.7.1.6 and 146.7.1.4.

146.7.1.1 Insertion loss

All 10BASE-T1L PHYs support the insertion loss specified in 146.7.1.1.2, but support of the insertion loss specified in 146.7.1.1.1 is required only when the 2.4 Vpp transmit/receive ability is operational.

146.7.1.1.1 Insertion loss for PHYs in the 2.4 Vpp operation mode

For PHYs in the 2.4 Vpp operation mode, the insertion loss of each 10BASE-T1L link segment shall meet the values determined using Equation (146–10).

$$\text{Insertion loss}(f) \le 10\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \qquad \text{(dB)} \qquad (146\text{–}10)$$

where

f is the frequency in MHz; $0.1 \le f \le 20$

The insertion loss is illustrated in Figure 146–26.

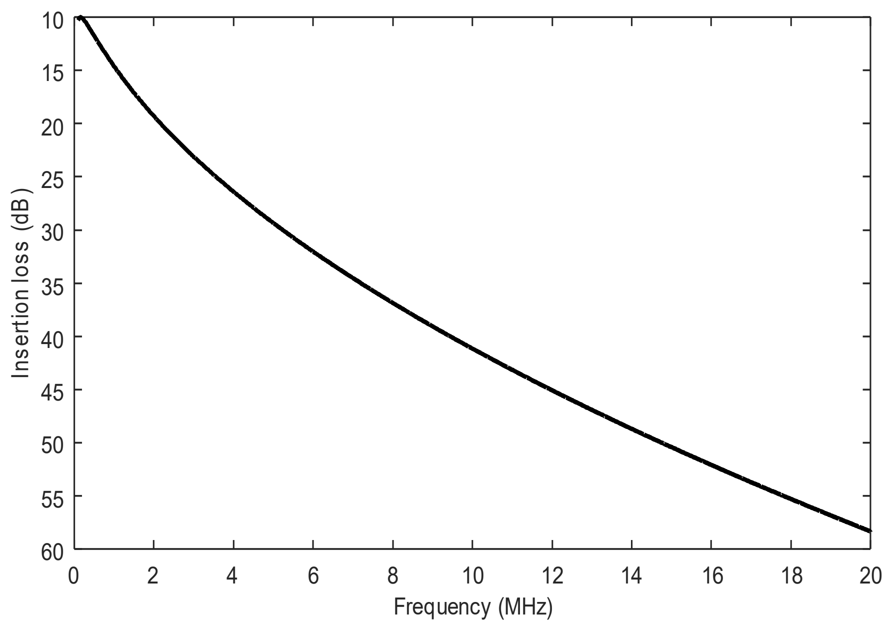


Figure 146–26—Insertion loss calculated using Equation (146–10)

146.7.1.1.2 Insertion loss supported for PHYs in 1.0 Vpp operation mode

For PHYs in the 1.0 Vpp operation mode, the insertion loss of each 10BASE-T1L link segment shall meet the values determined using Equation (146–11).

$$\text{Insertion loss}(f) \le 5.9\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \quad \text{(dB)} \qquad (146\text{–}11)$$

where

f is the frequency in MHz; $0.1 \le f \le 20$

The insertion loss is illustrated in Figure 146–27.

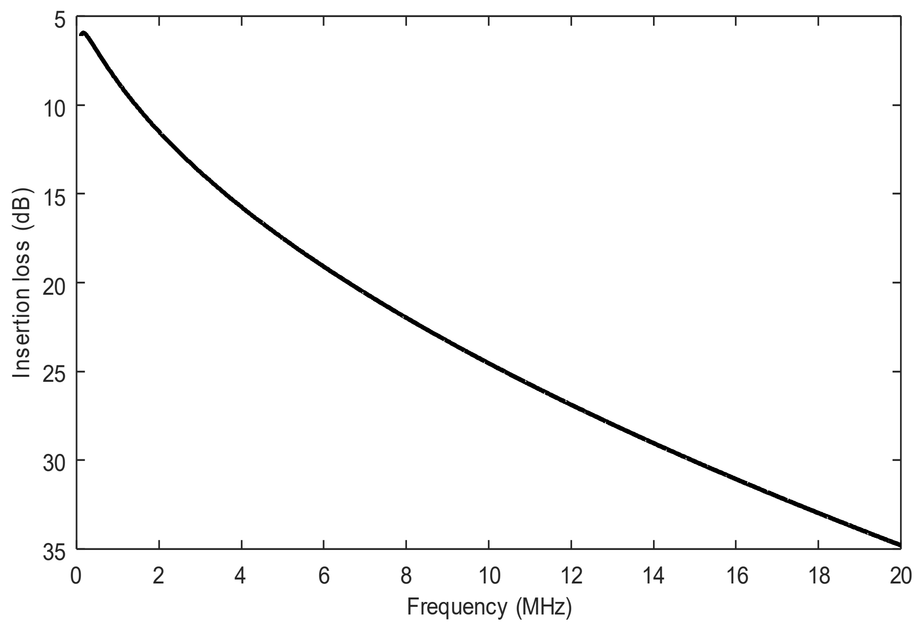


Figure 146–27—Insertion loss calculated using Equation (146–11)

146.7.1.2 Return loss

In order to limit the noise at the receiver due to impedance mismatches, each 10BASE-T1L link segment shall meet the values determined using Equation (146–12) at all frequencies from 0.1 MHz to 20 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return loss} \ge \begin{Bmatrix} 9 + 8 \times f & 0.1 \le f < 0.5 \text{ MHz} \\ 13 & 0.5 \le f \le 20 \text{ MHz} \end{Bmatrix} \text{dB} \qquad (146\text{–}12)$$

where

f is the frequency in MHz; $0.1 \le f \le 20$

The return loss is illustrated in Figure 146–28.

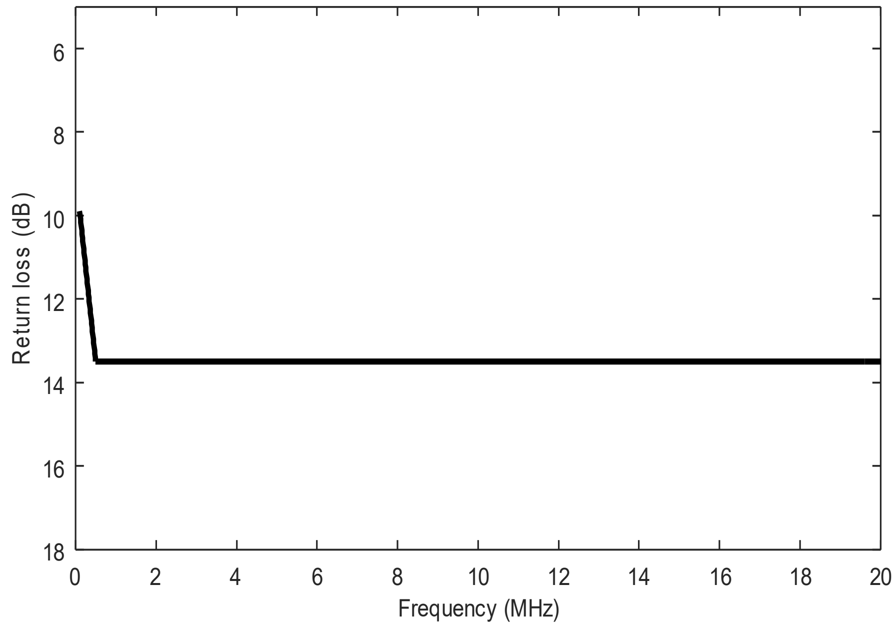


Figure 146–28—Return loss calculated using Equation (146–12)

146.7.1.3 Maximum link delay

The propagation delay of a 10BASE-T1L link segment shall not exceed 8834 ns at all frequencies between 0.1 MHz and 20 MHz. Note that the delay is derived from the point-to-point 1.63 mm (14 AWG) link segment length of 1589 m given in Table 146B–1 using Equation (80-1) with an ‘n’ of 0.6.

146.7.1.4 Differential to common mode conversion

The differential to common mode conversion requirement applies to unshielded link segments and depends on the electromagnetic noise environment. The requirements of Table 146–5 shall be met based on the local environment as described by the electromagnetic classifications given in Table 146–7, E_1 or E_2.

Table 146–5—Differential to common mode conversion

	Frequency (MHz)	E_1	E_2
TCL	$0.1 \le f \le 10$	≥ 50 dB	≥ 50 dB
TCL	$10 < f \le 20$	$\ge 50 - 20\log_{10}\left(\frac{f}{10}\right)$ dB	$\ge 50 - 20\log_{10}\left(\frac{f}{10}\right)$ dB

146.7.1.5 Coupling attenuation

The coupling attenuation requirement applies to shielded link segments and depends on the electromagnetic noise environment. The requirements in Table 146–6 shall be met based on the local environment as described by the electromagnetic classifications given in Table 146–7, E1, E2, or E3.

Table 146–6—Coupling attenuation

Frequency (MHz)	(dB)		
	E_1	E_2	E_3
0.1 to 20	≥ 50	≥ 50	≥ 60

146.7.1.6 Electromagnetic classifications

Electromagnetic classifications for the link segment local environments are given in Table 146–7, for E_1, E_2, or E_3.

Table 146–7—Link segment electromagnetic classifications (ISO/IEC 11801-1)

Electromagnetic	E_1	E_2	E_3
Conducted RF	3 V at 150 kHz to 80 MHz	3 V at 150 kHz to 80 MHz	10 V at 150 kHz to 80 MHz

146.7.2 Coupling parameters between 10BASE-T1L link segments

Noise coupled between the disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments is referred to as alien crosstalk noise. To ensure that the total alien NEXT loss and alien FEXT loss coupled between 10BASE-T1L link segments are limited, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien far-end crosstalk (MDAFEXT) loss are specified.

146.7.2.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

In order to limit the alien crosstalk at the near end of a 10BASE-T1L link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments is specified to meet the bit error ratio objective. To ensure that the total alien NEXT coupled into a 10BASE-T1L link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 0.1 MHz to 20 MHz as follows in Equation (146–13).

$$\mathrm{PSANEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN}(f)_{j,N}}{10}} \text{ dB} \qquad (146\text{–}13)$$

where the function $\mathrm{AN}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing 10BASE-T1L link segment j (1 to m) for the disturbed 10BASE-T1L link segment N.

The power sum ANEXT loss between a disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments shall meet the values determined using Equation (146–14) or 60 dB, whichever is less.

$$\mathrm{PSANEXT}(f) \geq 37.5 - 17\log_{10}\left(\frac{f}{20}\right)\ \mathrm{dB} \tag{146–14}$$

where

f is the frequency in MHz; $0.1 \leq f \leq 20$

146.7.2.2 Multiple disturber power sum alien far-end crosstalk (PSAFEXT) loss

In order to limit the alien crosstalk at the far-end of a 10BASE-T1L link segment, the differential pair-to-pair alien far-end crosstalk (FEXT) loss between the disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments is specified to meet the bit error ratio objective. To ensure that the total alien FEXT coupled into a 10BASE-T1L link segment is limited, multiple disturber AFEXT is specified as the power sum of the individual alien FEXT disturbers. Note that the MDAFEXT is specified as the power sum of the individual alien FEXT disturbers (PSAFEXT) and not individual alien ACRF disturbers (PSAACR-F).

PSAFEXT is determined by summing the power of the individual pair-to-pair differential alien FEXT values over the frequency range 0.1 MHz to 20 MHz as follows in Equation (146–15).

$$\mathrm{PSAFEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AF}(f)_{j,N}}{10}}\ \mathrm{dB} \tag{146–15}$$

where the function $\mathrm{AF}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien FEXT of the disturbing 10BASE-T1L link segment j (1 to m) for disturbed 10BASE-T1L link segment N.

The power sum AFEXT between a disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments shall meet the values determined using Equation (146–16) or 60 dB, whichever is less.

$$\mathrm{PSAFEXT}(f) \geq 38 - 18\log_{10}\left(\frac{f}{20}\right)\ \mathrm{dB} \tag{146–16}$$

where

f is the frequency in MHz; $0.1 \leq f \leq 20$

146.8 MDI specification

This subclause describes connectors that may be used at the MDI. It also specifies electrical requirements, including fault tolerance, at the MDI.

146.8.1 MDI connectors

The mechanical interface to the balanced cabling is a 3-pin connector (BI_DA+, BI_DA–, and optional SHIELD) or alternatively a 2-pin connector with an optional additional mechanical shield connection that conforms to the link segment specification defined in 146.7.

Specific systems or applications can use connectors or terminals that support the link segment specification defined in 146.7.

Connectors meeting the mechanical requirements of IEC 63171-1 [B39a] or IEC 63171-6:2020 [B39b] may be used as the mechanical interface to the balanced cabling. The plug connector is used on the balanced cabling and the MDI jack connector on the PHY. The IEC 63171-1 plug and jack are depicted (for informational use only) in Figure 146–29 and Figure 146–30 respectively, and the mating interface is depicted in Figure 146–31. The IEC 63171-6 plug and jack are depicted (for informational use only) in Figure 146–32 and Figure 146–33 respectively, and the mating interface is depicted in Figure 146–34. These connectors should support link segment DCR characteristics for 1.02 mm (18 AWG) to 0.40 mm (26 AWG) in Table 146B–1.

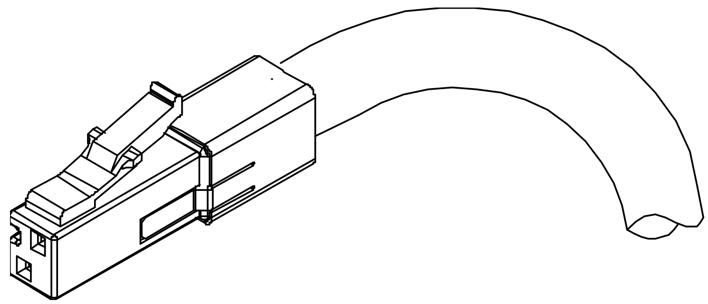


Figure 146–29—IEC 63171-1 plug

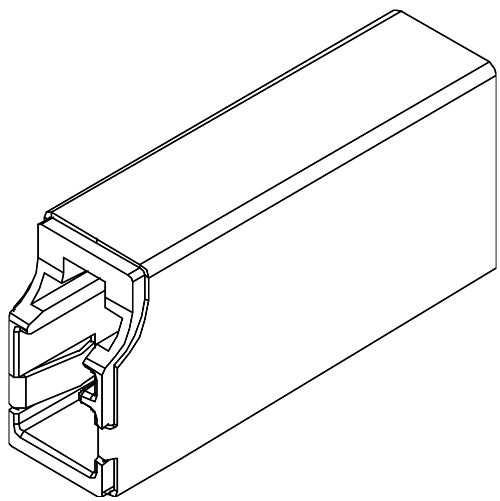


Figure 146–30—IEC 63171-1 jack

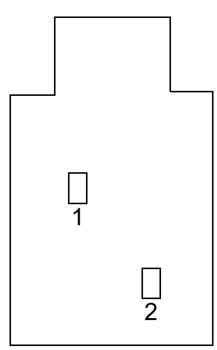


Figure 146–31—IEC 63171-1 mating face

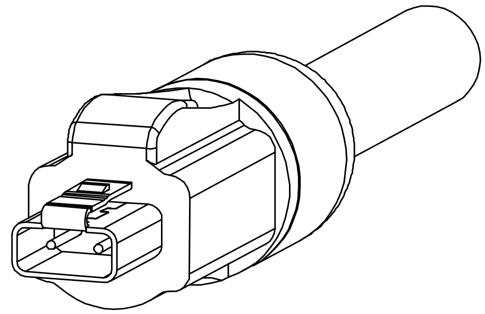


Figure 146–32—IEC 63171-6 plug

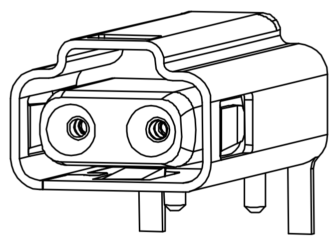


Figure 146–33—IEC 63171-6 jack

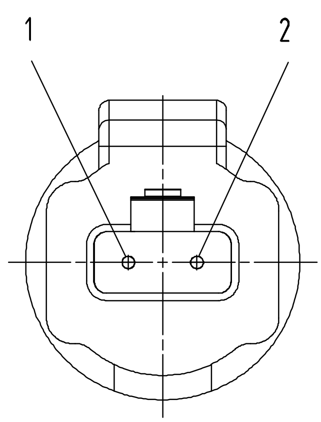


Figure 146–34—IEC 63171-6 mating face

The assignment of PMA signals to connector contacts for PHYs are given in Table 146–8.

Table 146–8—Assignment of PMA signals to MDI contacts

Contact	PMA signal
1	BI_DA+
2	BI_DA–

146.8.2 MDI electrical specification

The electrical requirements specified in 146.5.4 and 146.5.5 shall be met when the PHY is connected to the MDI connector mated with the specified plug connector.

146.8.3 MDI return loss

The MDI return loss (RL) shall meet or exceed Equation (146–17) for all frequencies from 100 kHz to 20 MHz (with 100 Ω ± 0.1% reference impedance) at all times when the PHY is transmitting data or idle symbols.

$$\text{Return Loss}(f) \geq \begin{cases} 20 - 18 \times \log_{10}\left(\frac{0.2}{f}\right) \text{ dB} & 0.1 \leq f < 0.2 \text{ MHz} \\ 20 \text{ dB} & 0.2 \leq f \leq 1 \text{ MHz} \\ 20 - 16.7 \times \log_{10}(f) \text{ dB} & 1 < f \leq 10 \text{ MHz} \\ 3.3 - 7.6 \times \log_{10}\left(\frac{f}{10}\right) \text{ dB} & 10 < f \leq 20 \text{ MHz} \end{cases} \quad (146\text{–}17)$$

where f is the frequency in MHz.

146.8.4 MDI mode conversion loss

Mode conversion LCL (Sdc11) or TCL (Scd11) of the PHY measured at the MDI shall meet the values determined using Equation (146–18).

$$\text{Conversion Loss}(f) \geq \begin{bmatrix} 25 \text{ dB} & 0.1 \leq f \leq 10 \text{ MHz} \\ 25 - 20 \times \log_{10}\left(\frac{f}{10}\right) \text{ dB} & 10 < f \leq 20 \text{ MHz} \end{bmatrix} \quad (146\text{–}18)$$

where f is the frequency in MHz.

146.8.5 MDI DC power voltage tolerance

The DTE shall withstand without damage the application of any voltages between 0 V dc and 60 V dc with the source current limited to 2000 mA, applied across BI_DA+ and BI_DA–, in either polarity, under all operating conditions, for an indefinite period of time. This requirement ensures that all devices tolerate DC powering voltages, such as those in Clause 104, even if the device does not require power.

146.8.6 MDI fault tolerance

The wire pair of the MDI shall withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, as per Table 146–9, under all operating conditions, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is/are removed.

The wire pair of the MDI is expected to withstand, without damage, high-voltage transient noises and ESD per application requirements. Table 146–9 gives an overview about possible connection faults for the wire pair (BI_DA+ and BI_DA–).

Table 146–9—Fault conditions

BI_DA+	BI_DA–
BI_DA–	BI_DA+
Ground	No fault
No fault	Ground
Ground	Ground
+60 V dc	No fault
No fault	+60 V dc
+60 V dc	+60 V dc
Ground	+60 V dc
+60 V dc	Ground

NOTE—Typically, industrial control circuits are SELV/PELV limited to a maximum voltage of 60 V. The maximum current is limited by the 50 Ω termination resistors in each signal line. Depending on the internal structure of the PHY IC, additional external clamping diodes could be necessary. Due to the AC signal coupling, the maximum current is applied only while charging the signal coupling capacitors.

146.9 Environmental specifications

146.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1, IEC 62368-1, or IEC 61010-1. All equipment subject to this clause may be additionally required to conform to any applicable local, state, or national standards

146.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. All 10BASE-T1L cabling is expected to be routed according to any applicable local, state, or national standards considering all relevant safety requirements.

146.9.2.1 Environmental safety

In industrial applications, all equipment subject to this clause is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications, where applicable:

— Environmental loads: IEC 60529 and ISO 4892
— Mechanical loads: IEC 60068-2-6 and IEC 60068-2-31
— Climatic loads: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-14, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, and IEC 60068-2-78

146.9.2.2 Electromagnetic compatibility

A system integrating the 10BASE-T1L PHY is expected to comply with all applicable local and national codes for electromagnetic compatibility.

146.10 Delay constraints

Every 10BASE-T1L PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the MDI, shall be less than 3.2 µs (32 bit times). The delay for the receive path, from the MDI to the MII output, shall be less than 6.4 µs (64 bit times).

146.11 Protocol implementation conformance statement (PICS) proforma for Clause 146, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L[1]

146.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 146, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

146.11.2 Identification

146.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

146.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cg-2019, Clause 146, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cg-2019.)	

Date of Statement	

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

146.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MII	PHY associated with MII	146.1.1		O	Yes [ ] No [ ]
*EEE	Energy Efficient Ethernet (EEE) capability	146.1.2, 78		O	Yes [ ] No [ ]
*AN	Auto-Negotiation	98		O	Yes [ ] No [ ]
*INS	Installation / cabling	146.7	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
PCS	10BASE-T1L PCS	146.3		M	Yes [ ]
PMA	10BASE-T1L PMA	146.4		M	Yes [ ]
*MDIO	MDIO capability	45.1		O	Yes [ ] No [ ]
*RTDL	2.4 Vpp operating mode	146.5.4.1		O	Yes [ ] No [ ]

146.11.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L

146.11.4.1 Physical Coding Sublayer (PCS)

146.11.4.1.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCST1	PCS reset	146.3.1	See 146.3.1	M	Yes [ ]
PCST2	PCS Data Transmission Enable function	146.3.2	Conform to the PCS Transmit State diagram	M	Yes [ ]
PCST3	PCS Transmit function	146.3.3.1	Conform to the PCS Transmit state diagram in Figure 146–5 and PCS Transmit multiplexer state diagram in Figure 146–6 and the associated state variables, functions, and messages	M	Yes [ ]
PCST4	Master PHY PCS side-stream scrambler	146.3.3.4.1	See Equation (146–1)	M	Yes [ ]
PCST5	Slave PHY PCS side-stream scrambler	146.3.3.4.1	See Equation (146–2)	M	Yes [ ]
PCST6	PCS scrambler seed values	146.3.3.4.1	Never initialized to zeros	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PCST7	$Sy_n[4:0]$	146.3.3.4.2	See 146.3.3.4.2	M	Yes [ ]
PCST8	$Sd_n[3:0]$	146.3.3.4.3	See 146.3.3.4.3	M	Yes [ ]
PCST9	$Sy_n[1]$ and $Sy_n[2]$	146.3.3.4.3	Swapped compared to data transmission	M	Yes [ ]

146.11.4.1.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PCSR1	PCS Receive function	146.3.4.1	Conform to the PCS Receive state diagram and associated variables	M	Yes [ ]
PCSR2	Receive watchdog state diagram	146.3.4.1	See Figure 146–11	M	Yes [ ]
PCSR3	Maximum dwelling time in DATA state of PCS receive state diagram	146.3.4.1	Less than rcv_max_timer	M	Yes [ ]
PCSR4	disparity_error signal	146.3.4.2	Generated by the decoder when a code-group is received that is not allowed according to the current running disparity value	M	Yes [ ]
PCSR5	RX_DV	146.3.4.2	RX_DV = TRUE when SSD is received, RX_DV = FALSE when ESD or ESD with error is received	M	Yes [ ]
PCSR6	RX_ER	146.3.4.2	RX_ER = TRUE when bad ESDs, ERR_ESD, or bad SSDs are received, RX_ER reset to FALSE when in IDLE state of PCS Receive state diagram	M	Yes [ ]
PCSR7	MASTER PHY side-stream descrambler	146.3.4.3	See Equation (146–4)	M	Yes [ ]
PCSR8	SLAVE PHY side-stream descrambler	146.3.4.3	See Equation (146–5)	M	Yes [ ]
PCSR9	Automatic polarity detection	146.3.4.4	Implemented in the PHY receiver	M	Yes [ ]

146.11.4.1.3 PCS loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCSL1	PCS loopback	146.3.5	The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, or the loopback bit in MDIO register 3.2278.14, defined in 45.2.3.68a.2, is set to one	MDIO:M	Yes [ ] N/A [ ]
PCSL2	PCS loopback function	146.3.5	The PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII	M	Yes [ ]
PCSL3	PHY receive circuitry isolation	146.3.5	The PHY receive circuitry shall be isolated from the network medium	M	Yes [ ]
PCSL4	PHY transmit circuity isolation	146.3.5	The assertion of TX_EN at the MII shall not result in the transmission of data on the network medium	M	Yes [ ]

146.11.4.2 Physical Medium Attachment (PMA)

146.11.4.2.1 PMA function

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	PMA reset function	146.4.1	See 146.4.1	M	Yes [ ]
PMA2	PMA reset	146.4.1	Set pma_reset = TRUE while reset conditions hold true	M	Yes [ ]
PMA3	PMA Transmit fault function	146.4.2	Mapped to the transmit fault bit as specified in 45.2.1.7.4	MDIO:O	Yes [ ] No [ ] N/A [ ]
PMA4	PMA Receive fault function	146.4.3	Contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.186b.7	MDIO:O	Yes [ ] No [ ] N/A [ ]
PMA5	LPI synchronization	146.4.4	EEE-capable PHYs synchronize refresh intervals during periods of low-power idle	EEE:M	Yes [ ] N/A [ ]
PMA6	PHY Control	146.4.4	See Figure 146–15, Figure 146–16, and Figure 146–17	M	Yes [ ]
PMA7	Link Monitor operation	146.4.5	See Figure 146–18	M	Yes [ ]
PMA8	Quiet-Refresh cycling state diagram	146.4.7	See Figure 146–19	EEE:M	Yes [ ] N/A [ ]

146.11.4.2.2 PMA electrical specification

Item	Feature	Subclause	Value/Comment	Status	Support
PMAE1	Test modes	146.5.2	Implemented in PHY to allow testing transmitter electrical requirements	M	Yes [ ]
PMAE2	Enable test modes	146.5.2	Enable by setting bits 1.2296.15:13 as described in 45.2.1.186c.1 when MDIO implemented; similar functionality provided otherwise	MDIO: M	Yes [ ] N/A [ ]
PMAE3	These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation	146.5.2		M	Yes [ ]
PMAE4	Test mode 1	146.5.2	When enabled, PHY repeatedly transmits the data symbol sequence (+1, –1)	M	Yes [ ]
PMAE5	Test mode 2	146.5.2	When enabled, PHY repeatedly transmits ten “+1” symbols followed by ten “–1” symbols	M	Yes [ ]
PMAE6	Test mode 3	146.5.2	Transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals	M	Yes [ ]
PMAE7	TX_TCLK	146.5.3	PHY to provide access to the symbol rate clock	M	Yes [ ]
PMAE8	AC coupling at MDI	146.5.4		M	Yes [ ]
PMAE9	The transmitter shall meet the requirements of this subclause with a 100 Ω ± 0.1% resistive differential load connected to the transmitter output	146.5.4		M	Yes [ ]
PMAE10	Transmitter output voltage	146.5.4.1	2.4 V + 5%/– 15% peak-to-peak in the 2.4 Vpp operating mode when measured on test mode 1, 1.0 V + 5%/– 15% peak-to-peak in the 1.0 Vpp operating mode when measured on test mode 1	RTDL: M	Yes [ ] N/A [ ]
PMAE11	Transmitter output droop	146.5.4.2	Less than 10%	M	Yes [ ]
PMAE12	Transmitter timing jitter	146.5.4.3	Less than 10 ns symbol-to-symbol jitter when measured on test mode 1	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PMAE13	Transmit power in test mode 3	146.5.4.4	8.6 ± 1.0 dBm for the 2.4 Vpp transmit amplitude, and 1 ± 1.2 dBm for the 1.0 Vpp transmit amplitude, when measured into a 100 Ω load using the test fixture shown in Figure 146–21	M	Yes [ ]
PMAE14	Transmit power spectral density in test mode 3	146.5.4.4	Between the upper and lower masks specified in Equation (146–6) and Equation (146–7) for the 2.4 Vpp transmit amplitude and Equation (146–8) and Equation (146–9) for the 1.0 Vpp transmit amplitude, when measured into a 100 Ω load using the test fixture shown in Figure 146–21	M	Yes [ ]
PMAE15	Transmitter clock frequency	146.5.4.5	Within the range of 7.5 MBd ± 50 ppm	M	Yes [ ]
PMAE16	LPI mode the short-term rate of frequency variation	146.5.4.5	Less than 0.1 ppm/second	EEE:M	Yes [ ] N/A [ ]
PMAE17	PMA receive function	146.5.5	Requirements met using link segment defined in 146.7	M	Yes [ ]
PMAE18	Receiver differential input signals	146.5.5.1	Received with a bit error ratio less than 10^{-9}	M	Yes [ ]
PMAE19	Receiver frequency tolerance	146.5.5.2	Within the range of 7.5 MBd ± 50 ppm	M	Yes [ ]
PMAE20	Alien crosstalk noise rejection	146.5.5.3	BER < 10^{-9} with an alien crosstalk noise of magnitude of –106 dBm/Hz and bandwidth of 10 MHz at the MDI	M	Yes [ ]
PMAE21	PMA local loopback	146.5.6	The PMA shall be placed in loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or in MDIO register 1.2294.0, defined in 45.2.1.186a.6 is set to one	MDIO:O	Yes [ ] No [ ] N/A [ ]

146.11.4.3 Management interface

Item	Feature	Subclause	Value/Comment	Status	Support
MI1	Auto-Negotiation	146.1.2, 146.6.1	Clause 98 is used if Auto-Negotiation is supported and enabled	AN:M	Yes [ ] N/A [ ]
MI2	MASTER-SLAVE relationship when Auto-Negotiation is not used	146.1.2	Established by management or hardware configuration of the PHYs	M	Yes [ ]
MI3	MASTER/SLAVE mode selection	146.6.3	Default setting chosen by Auto-Negotiation, by setting bits 1.2100.14 as described in 45.2.1.185 when MDIO is implemented; similar functionality provided otherwise	AN:M MDIO:M	Yes [ ] N/A [ ]
MI4	Transmitter output voltage setting	146.6.4	Default setting chosen by Auto-Negotiation, by setting bit 1.2294.12 as described in 45.2.1.186a.3 when MDIO implemented; similar functionality provided otherwise	RTDL:O	Yes [ ] No [ ] N/A [ ]
MI5	Increased transmit level request	146.6.4	Bit A23 contains a one if the PHY is requesting the increased transmit level; otherwise, bit A23 contains a zero	RTDL:O AN:M	Yes [ ] No [ ] N/A [ ]
MI6	Increased transmit level support	146.6.4	Bit A24 contains a one if the PHY is supporting and advertising the 2.4 Vpp operating mode; otherwise, bit A24 contains a zero	RTDL:O AN:M	Yes [ ] No [ ] N/A [ ]
MI7	Increased transmit level selection	146.6.4	If both PHYs advertise increased transmit/receive ability and at least one PHY requests an increased transmit level, the 2.4 Vpp operating mode is selected; otherwise, the 1.0 Vpp operating mode is selected	RTDL:O AN:M	Yes [ ] No [ ] N/A [ ]
MI8	Energy Efficient Ethernet ability	146.6.5	Bit A25 contains a one if Energy Efficient Ethernet is supported and advertised; otherwise, bit A25 contains a zero	EEE:M AN:M	Yes [ ] N/A [ ]
MI9	PMA and PCS MDIO function mapping	146.6.6	See Table 146–4 when MDIO is implemented; similar functionality provided otherwise	MDIO:M	Yes [ ] N/A [ ]

146.11.4.4 Link Segment characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
LMF1	Insertion loss (1.0 Vpp operating mode)	146.7.1.1.2	See Equation (146–11)	INS:M	Yes [ ]
LMF2	Insertion loss (2.4 Vpp operating mode)	146.7.1.1.1	See Equation (146–10)	INS:O, RTDL:M	Yes [ ] N/A[]
LMF3	Return loss	146.7.1.2	See Equation (146–12)	INS:M	Yes [ ]
LMF4	Maximum link delay	146.7.1.3	Not exceed 8834 ns for all frequencies between 1 MHz to 20 MHz	INS:M	Yes [ ]
LMF5	Differential to common mode conversion	146.7.1.4	See Table 146–5	INS:M	Yes [ ]
LMF6	Coupling attenuation	146.7.1.5	See Table 146–6	INS:M	Yes [ ]
LMF7	Power sum ANEXT loss between a disturbed 10BASE-T1L link segment and the disturbing 10BASE-T1L link segment	146.7.2.1	See Equation (146–14) or 60 dB, whichever is less	INS:M	Yes [ ]
LMF8	Power sum AFEXT loss between a disturbed 10BASE-T1L link segment and the disturbing 10BASE-T1L link segment	146.7.2.2	See Equation (146–16) or 60 dB, whichever is less	INS:M	Yes [ ]

146.11.4.5 MDI specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	Mated MDI performance	146.8.2	Electrical requirements specified in 146.5.4 and 146.5.5 shall be met when the PHY is connected to the MDI connector mated with the specified plug connector	M	Yes [ ]
MDI2	MDI Return Loss	146.8.3	Meets or exceeds Equation (146–17)	M	Yes [ ]
MDI3	MDI Mode conversion loss	146.8.4	Meets or exceeds Equation (146–18)	M	Yes [ ]
MDI4	MDI line powering voltage tolerance	146.8.5	Up to 60 V DC with the source current limited to 2000 mA	M	Yes [ ]
MDI5	MDI fault tolerance	146.8.6	Withstand without damage the application of a short circuit of any wire to the other wire of the same pair or ground potential, operation resumes after removing the short(s)	M	Yes [ ]

146.11.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Conform to IEC 60950-1, IEC 62368-1, or IEC 61010-1	146.9.1		M	Yes [ ]

146.11.4.7 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	10BASE-T1L PHY associated with MII	146.10	Comply with the bit delay constraints for full duplex operation	M	Yes [ ]
DC2	Transmit path delay	146.10	Less than 3.2 μs (32 bit times)	M	Yes [ ]
DC3	Receive path delay	146.10	Less than 6.4 μs (64 bit times)	M	Yes [ ]

147. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S

147.1 Overview

This clause defines the type 10BASE-T1S Physical Coding Sublayer (PCS) and type 10BASE-T1S Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 10BASE-T1S Physical Layer (PHY). Provided in this clause are full functional and electrical specifications for the type 10BASE-T1S PCS, PMA, and MDI.

The 10BASE-T1S PHY is specified to be capable of operating at 10 Mb/s in several modes. All 10BASE-T1S PHYs can operate as a half-duplex PHY with a single link partner over a point-to-point link segment defined in 147.7, and, additionally, there are two mutually exclusive optional operating modes: a full-duplex point-to-point mode over the link segment, defined in 147.7, and a half-duplex shared-medium mode, referred to as multidrop mode, capable of operating with multiple stations connected to a mixing segment, defined in 147.8. The medium supporting the operation of the 10BASE-T1S PHY is defined in terms of performance requirements between the attachment points (Medium Dependent Interface (MDI)), allowing implementers to specify their own media to operate the 10BASE-T1S PHY as long as the normative requirements included in this clause are met.

10BASE-T1S PHYs optionally support PHY Level Collision Avoidance (PLCA), described in Clause 148.

10BASE-T1S follows an integrated PCS and PMA architecture and therefore does not support an AUI (see Figure 1–1).

147.1.1 Relationship of 10BASE-T1S to other standards

The relationship between the 10BASE-T1S, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet model are shown in Figure 147–1. The PHY sublayers (shown shaded) in Figure 147–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 10BASE-T1S is defined in Clause 98 and is not available in multidrop mode. Selection between multidrop and point-to-point mode is made via the appropriate configuration bit. A Management Entity is required using MDIO or equivalent functionality. Optional MDIO is defined in Clause 45.

147.1.2 Operation of 10BASE-T1S

All 10BASE-T1S PHYs can operate using half-duplex point-to-point communications on a link segment using a single balanced pair of conductors, supporting up to four in-line connectors and up to at least 15 meters in reach, with an effective data rate of 10 Mb/s shared between the two directions of transmission. 10BASE-T1S PHYs supporting the option of full-duplex point-to-point operation may operate with an effective data rate of 10 Mb/s in each direction simultaneously, supporting up to four in-line connectors and up to at least 15 meters in reach.

Additionally, the 10BASE-T1S PHY may operate using half-duplex communications on a mixing segment using a single balanced pair of conductors, interconnecting up to at least 8 PHYs to a trunk up to at least 25 m. PHYs may be attached in-line with the trunk or at the end of stubs with a length of up to 10 cm. An overall effective data rate of 10 Mb/s is shared among the nodes. Larger PHY count and reach may be achieved provided the mixing segment specifications in 147.8 are met.

The 10BASE-T1S PHY utilizes two level Differential Manchester Encoding (DME). A 17-bit self-synchronizing scrambler is used to improve the EMC performance. Following scrambling of the data, 4B/5B encoding is performed (see 147.3.2.4). DME is a self-clocked and intrinsically balanced line coding that guarantees very low DC baseline wander and allows for robust clock and data recovery in noisy environments. The 4B/5B mapping and the scrambler are contained within the PCS (see 147.3) while the DME encoder/decoder is contained in the PMA (see 147.4).

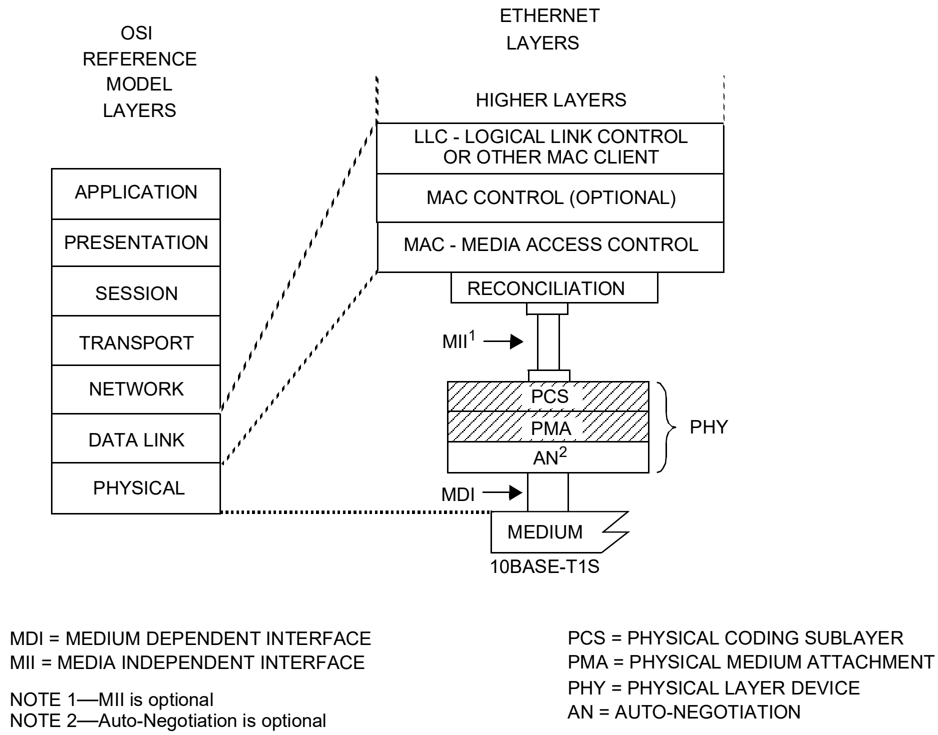


Figure 147–1—Relationship of 10BASE-T1S PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

147.1.3 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

147.1.3.1 State diagram notation

The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE, all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE, the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

147.1.3.2 State diagram timer specifications

All timers operate in the manner described in 40.4.5.2.

147.1.3.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

147.2 Service primitives and interfaces

The 10BASE-T1S PHY uses the service primitives and interfaces in 40.2, with exception of the following clarifications and differences noted in this subclause. Figure 147–2 shows the relationship of the service primitives and interfaces used by the 10BASE-T1S PHY.

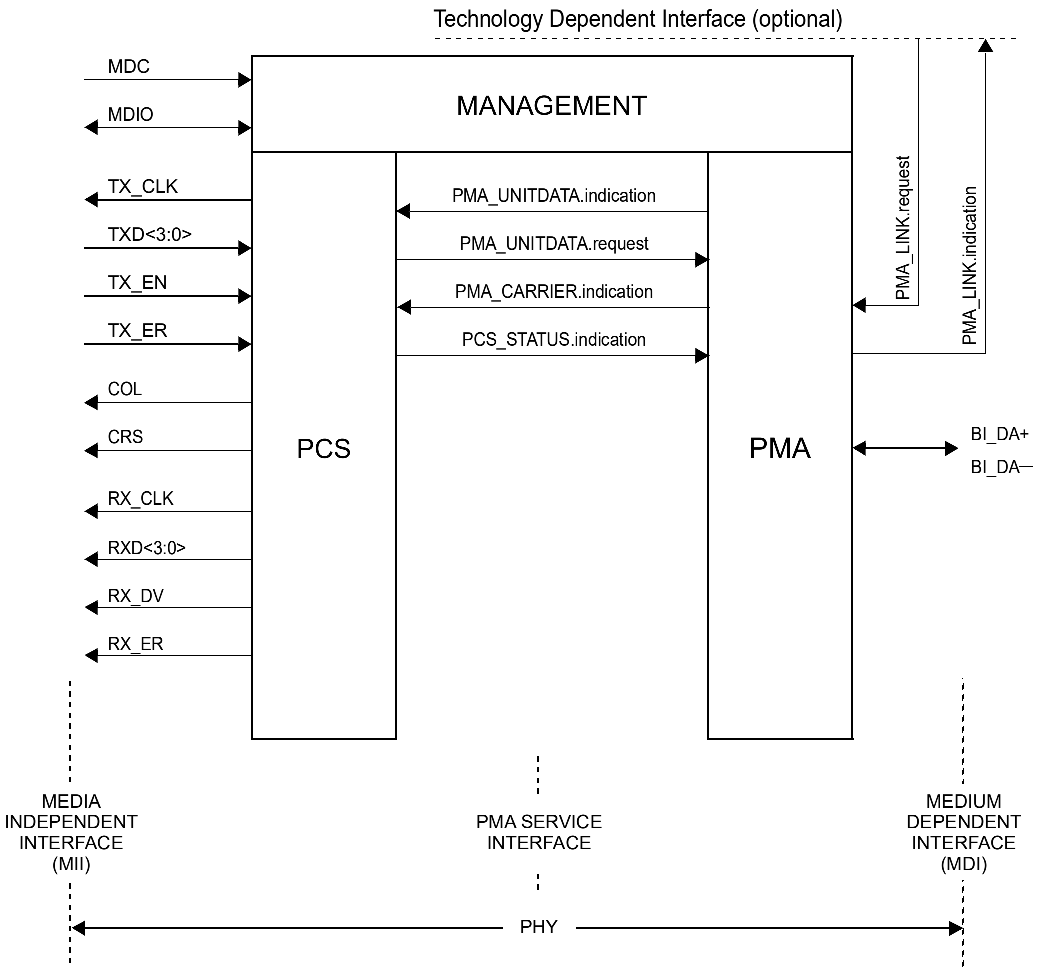


Figure 147–2—10BASE-T1S PHY interfaces

The 10BASE-T1S PHY uses the Media Independent Interface (MII) as specified in Clause 22.

As shown in Figure 147–2, 10BASE-T1S uses the following service primitives to exchange symbol vectors, status indications, and control signals across the PMA service interface:

PMA_UNITDATA.indication (rx_sym)
PMA_UNITDATA.request (tx_sym)
PMA_CARRIER.indication (pma_crs)
PMA_LINK.indication (link_status)

PMA_LINK.request (link_control)
PCS_STATUS.indication (pcs_status)

147.2.1 PMA_UNITDATA.indication

This primitive defines the transfer of one 5B symbol in the form of the rx_sym parameter from the PMA to the PCS.

147.2.1.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_sym)

During reception, the PMA_UNITDATA.indication conveys to the PCS, via the parameter rx_sym, the value of the 5B symbol detected on the MDI during each cycle of the recovered clock.

147.2.1.2 When generated

The PMA generates PMA_UNITDATA.indication (rx_sym) messages synchronously for every 5B symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 2.5 MHz, as governed by the recovered clock.

147.2.1.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

147.2.2 PMA_UNITDATA.request

This primitive defines the transfer of one symbol in the form of the tx_sym parameter from the PCS to the PMA.

The symbol is obtained in the PCS Transmit function using the encoding rules defined in 147.3.2 to represent 4B/5B encoded MII data or special out of band signaling.

147.2.2.1 Semantics of the primitive

PMA_UNITDATA.request (tx_sym)

During transmission, the PMA_UNITDATA.request conveys the value of the symbol to be sent over the MDI, via the parameter tx_sym.

The tx_sym parameter is one of the allowed 5B codes specified in Table 147–1.

147.2.2.2 When generated

The PCS generates PMA_UNITDATA.request (tx_sym) synchronously with every symb_timer expiration. The symb_timer is defined in 147.3.2.6.

147.2.2.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated 5B symbol after processing it with DME following the rules in 147.4.

147.2.3 Mapping of PMA_CARRIER.indication

Reports whether a signal compatible with DME encoding rules specified in 147.4.2 is detected on the medium.

147.2.3.1 Function

Maps the primitive PMA_CARRIER.indication to the MII CRS signal.

147.2.3.2 Semantic of the service primitive

PMA_CARRIER.indication (pma_crs)

The pma_crs parameter can take one of two values: CARRIER_ON or CARRIER_OFF.

The pma_crs parameter is set to CARRIER_ON if a signal compatible with DME encoding rules specified in 147.4.2 is present on the medium. Otherwise, the pma_crs parameter is set to CARRIER_OFF.

147.2.3.3 When generated

The PMA_CARRIER.indication primitive is generated continuously by the PMA sublayer.

147.2.4 PMA_LINK.request

This primitive allows Auto-Negotiation to enable and disable operation of the PMA, as specified in 98.4.2.

147.2.4.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of the following two values:

DISABLE	Used by Auto-Negotiation function to disable the PHY.
ENABLE	Used by Auto-Negotiation function to enable the PHY.

147.2.4.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

147.2.5 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs Auto-Negotiation functions about the status of the underlying link.

147.2.5.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on the following two values:

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 10BASE-T1S link is established. Reliable reception of signals transmitted from the remote PHY is possible.

147.2.5.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 147–14.

147.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

147.2.6 PCS_STATUS.indication

This primitive is generated by the PCS to indicate PCS status to the PMA.

147.2.6.1 Semantics of the primitive

PCS_STATUS.indication (pcs_status)

The pcs_status parameter can take on the following two values:

NOT_OK	PCS is not receiving valid packets or heartbeat signals from the remote PHY.
OK	PCS is actively receiving valid packets and/or heartbeat signals from the remote PHY.

147.2.6.2 When generated

The PCS generates this primitive continuously. The pcs_status parameter is set according to the state diagram in Figure 147–11.

147.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 147.4.4.

147.3 Physical Coding Sublayer (PCS) functions

The Physical Coding Sublayer (PCS) consists of PCS Reset, PCS Transmit, and PCS Receive functions as shown in Figure 147–3. The PCS Reset function is explained in 147.3.1, the PCS Transmit function is explained in 147.3.2, the PCS Receive function is explained in 147.3.3, and the PCS Loopback function is explained in 147.3.4.

147.3.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever any of the following conditions occur:

a) Power on causes power_on = TRUE (see 36.2.5.1.3) while pcs_reset = FALSE.
b) The receipt of a request for reset from the management entity (bit 3.2291.15 defined in 45.2.3.68c.1), independently from the current state of pcs_reset.

All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. PCS Reset shall keep pcs_reset = TRUE until the complete execution of the PCS Reset function, after which it is set to pcs_reset = FALSE. The reference diagrams do not explicitly show the PCS Reset function.

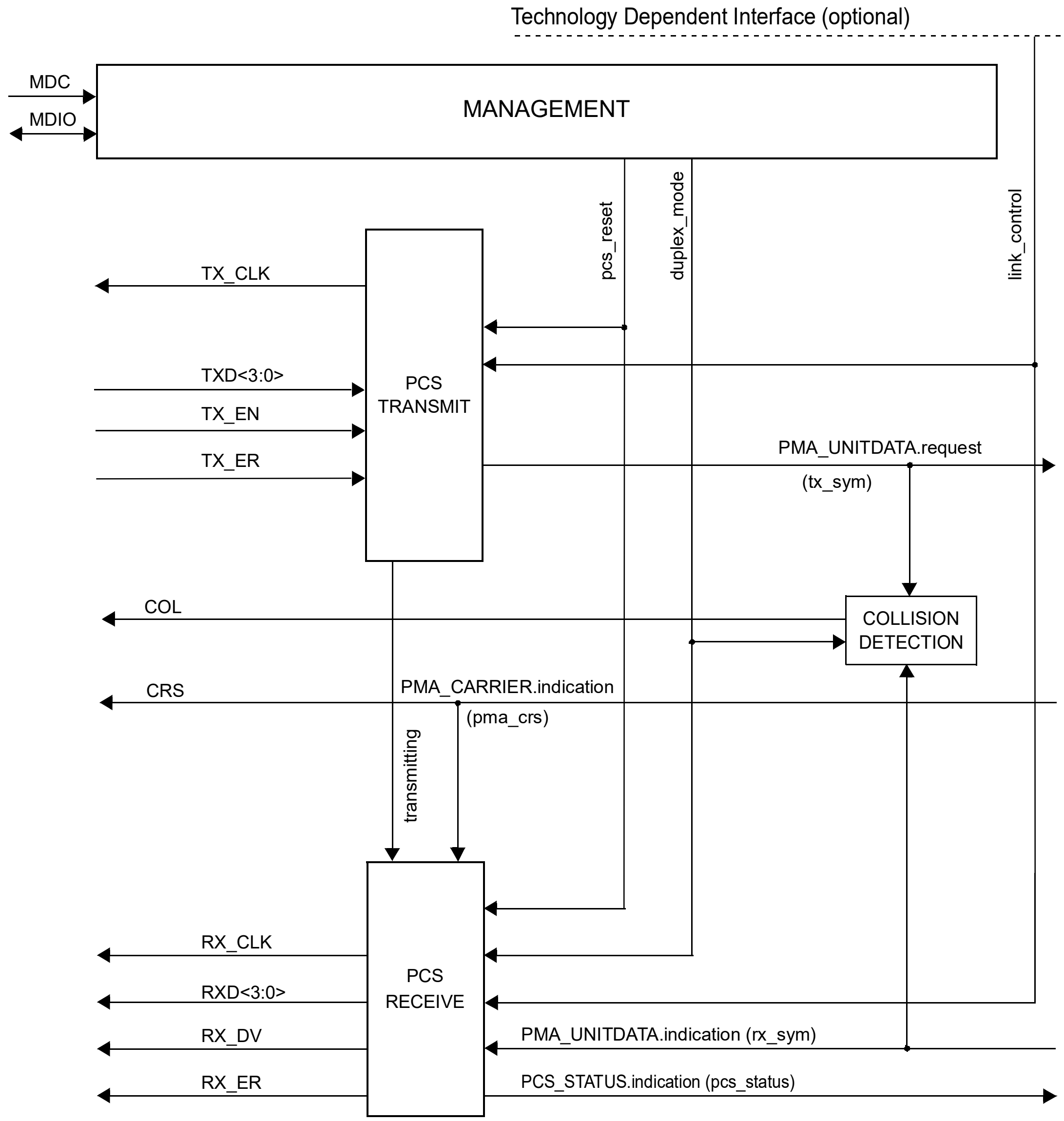


Figure 147–3—PCS reference diagram

147.3.2 PCS Transmit

147.3.2.1 PCS Transmit overview

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 147–4 and Figure 147–5, and the associated state variables, functions, timers, and messages.

At each symbol period, PCS Transmit generates a symbol tx_sym conveyed to the PMA through the PMA_UNITDATA.request service primitive, where tx_sym is a 5B symbol. The PMA encodes tx_sym, LSB first, into a DME stream over the wire pair BI_DA as specified in Table 147–2.

Upon assertion of TX_EN, the PCS Transmit function passes two SYNC symbols to the PMA, followed by two SSD symbols that replace the first 16 bits of the packet preamble. Following the second SSD, TXD<3:0> is encoded into 5B symbols using the encoding rules specified in Table 147–1, until TX_EN is deasserted.

Following the deassertion of TX_EN, the PCS Transmit generates a special code ESD. When there is no transmit error, ESD is followed by ESDOK. When there is a transmit error, ESD is followed by ESDERR. When a jabber condition is detected, ESD is followed by ESDJAB.

The 10BASE-T1S PHY has one special 5B symbol 'I' (see Table 147–1) which represents SILENCE. SILENCE represents an indication for the PMA to change the output according to 147.4.2.

147.3.2.2 Variables

err

This variable is set in the PCS Transmit state, as described in Figure 147–4 and Figure 147–5.
This variable is used to detect and latch a TX_ER = TRUE condition during data transmission; if such error is detected, an ESDERR symbol is sent at the end of transmission.
Values: TRUE or FALSE

hb_cmd

See 147.3.7.1.1.

link_control

This variable is generated by the Auto-Negotiation function. When Auto-Negotiation is not present or Auto-Negotiation is disabled, link_control has a default value of ENABLE, and may be provided by implementation-dependent functionality. When set to DISABLE, all PCS functions are switched off and no data can be sent or received.
Values: ENABLE or DISABLE

pcs_reset

The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

TX_EN

The TX_EN signal of the MII as specified in 22.2.2.3.
When set to FALSE transmission is disabled.
When set to TRUE transmission is enabled.
Values: TRUE or FALSE

TX_ER

The TX_ER signal of the MII as specified in 22.2.2.5.
When set to FALSE it indicates a non-errored transmission.
When set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

TXD

The TXD signal of the MII as specified in 22.2.2.4.
This signal represents a 4B data nibble to be transmitted.

tx_cmd

Encoding present on TXD<3:0>, TX_ER, and TX_EN as defined in Table 22–1.
Values:
BEACON: PLCA BEACON indication encoding present on TXD<3:0>, TX_ER, and TX_EN.
COMMIT: PLCA COMMIT indication encoding present on TXD<3:0>, TX_ER, and TX_EN.
SILENCE: TXD<3:0> does not encode any of the above requests, or TX_ER = FALSE, or TX_EN = TRUE.

tx_sym

5B symbol to be conveyed to the PMA Transmit function by the means of the PMA_UNITDATA.request primitive specified in 147.2.2.

transmitting

This variable is set in the PCS Transmit state, as described in Figure 147–4.
When this variable is set to TRUE, it indicates a transmission is ongoing.
Values: TRUE or FALSE

147.3.2.3 Constants

SYNC / COMMIT

5B symbol defined as 'J' in 4B/5B encoding.

SSD

5B symbol defined as 'H' in 4B/5B encoding.

ESD

5B symbol defined as 'T' in 4B/5B encoding.

ESDERR

5B symbol defined as 'K' in 4B/5B encoding.

ESDOK / ESDBRS

5B symbol defined as 'R' in 4B/5B encoding.

SILENCE

5B symbol defined as 'I' in 4B/5B encoding.

ESDJAB

5B symbol defined as 'S' in 4B/5B encoding.

147.3.2.4 Functions

ENCODE

This function takes a 4 bit input parameter Sc_n<3:0> and returns a 5B symbol according to the following procedure:

1. Convert Sc_n<3:0> into Sd_n<3:0> as specified in 147.3.2.8.
2. Convert Sd_n<3:0> (4B symbol) into the corresponding 5B symbol defined in Table 147–1.

Table 147–1—4B/5B Encoding

Name	4B	5B	Special function
0	0000	11110	—
1	0001	01001	—
2	0010	10100	—
3	0011	10101	—
4	0100	01010	—
5	0101	01011	—
6	0110	01110	—
7	0111	01111	—
8	1000	10010	—
9	1001	10011	—
A	1010	10110	—
B	1011	10111	—
C	1100	11010	—
D	1101	11011	—
E	1110	11100	—
F	1111	11101	—
I	N/A	11111	SILENCE
J	N/A	11000	SYNC / COMMIT
K	N/A	10001	ESDERR
T	N/A	01101	ESD / HB
R	N/A	00111	ESDOK / ESDBRS
H	N/A	00100	SSD
N	N/A	01000	BEACON
S	N/A	11001	ESDJAB

TXCMD_ENCODE

In the PCS transmit process, this function takes as its arguments the values of tx_cmd and hb_cmd variables and returns a 5B symbol based on the following mapping:
'N' when the tx_cmd variable is set to BEACON,
'J' when the tx_cmd variable is set to COMMIT,
'T' when the hb_cmd variable is set to HEARTBEAT and the tx_cmd variable is not set to BEACON or COMMIT,
'I' otherwise.

147.3.2.5 Abbreviations

STD Alias for symb_timer_done.

147.3.2.6 Timers

symb_timer

A continuous free-running timer. PMA_UNITDATA.request messages are issued by the PCS concurrently with symb_timer_done (see 147.2.2). TX_CLK (see 22.2.2.1) shall be generated from symb_timer with the rising edge of TX_CLK generated synchronously with symb_timer_done.
Continuous timer: The condition symb_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration.
Duration: 400 ns ± 100 ppm (see 22.2.2.1)

unjab_timer

Optionally times the minimum duration the PHY suppresses any transmission before reverting to normal operations.
Duration: 16 ms ± 100 µs

xmit_max_timer

Defines the maximum time the PCS Transmit state diagram can stay in DATA state.
The xmit_max_timer shall be implemented in such a way that, upon expiration, an even number of nibbles has been sent to prevent the MAC from counting false alignment errors.
Duration: 2 ms ± 100 µs

NOTE—This is approximately 25% greater than maxEnvelopeFrameSize specified in 4.2.7.1.

147.3.2.7 State diagram

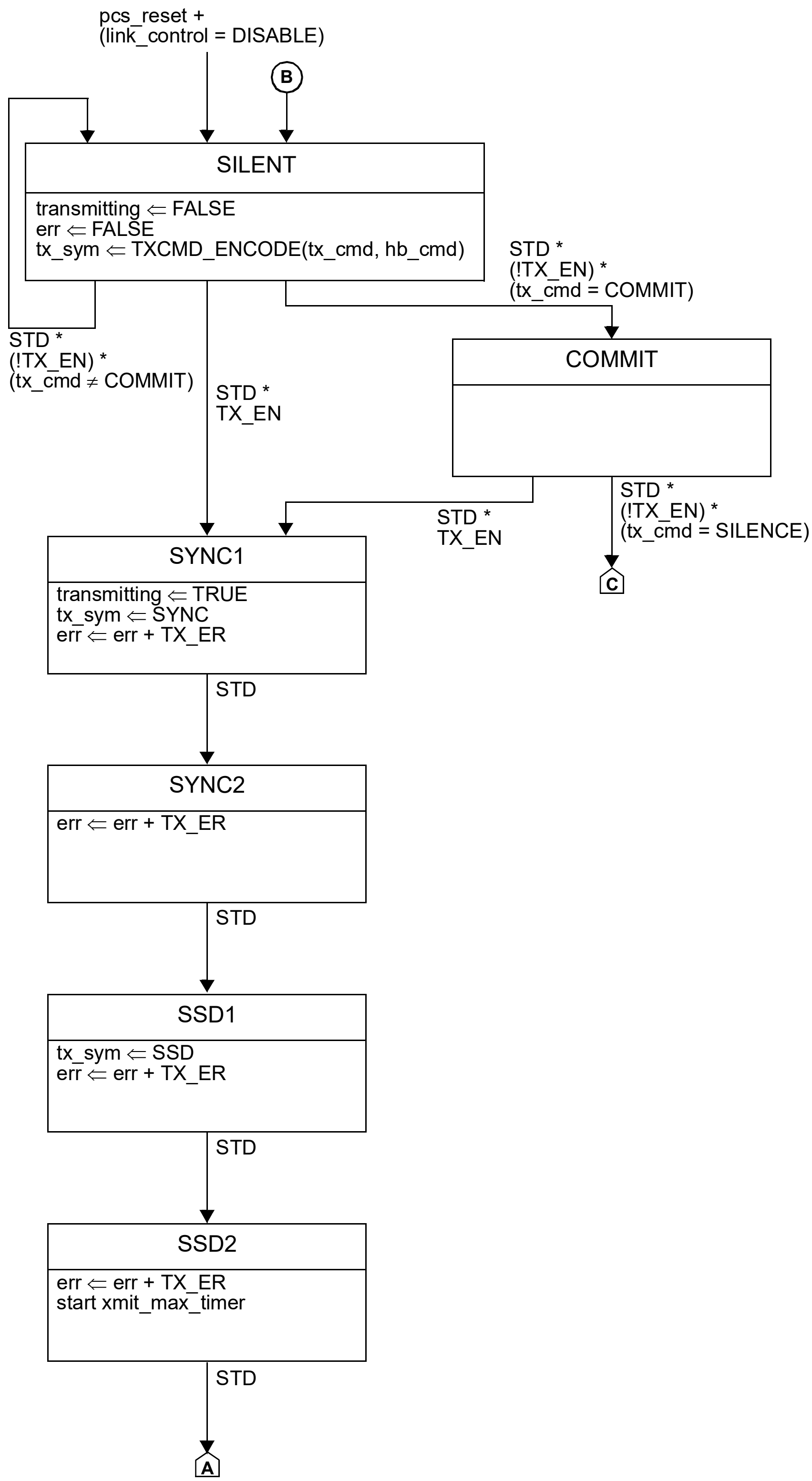


Figure 147–4—PCS Transmit state diagram, part a

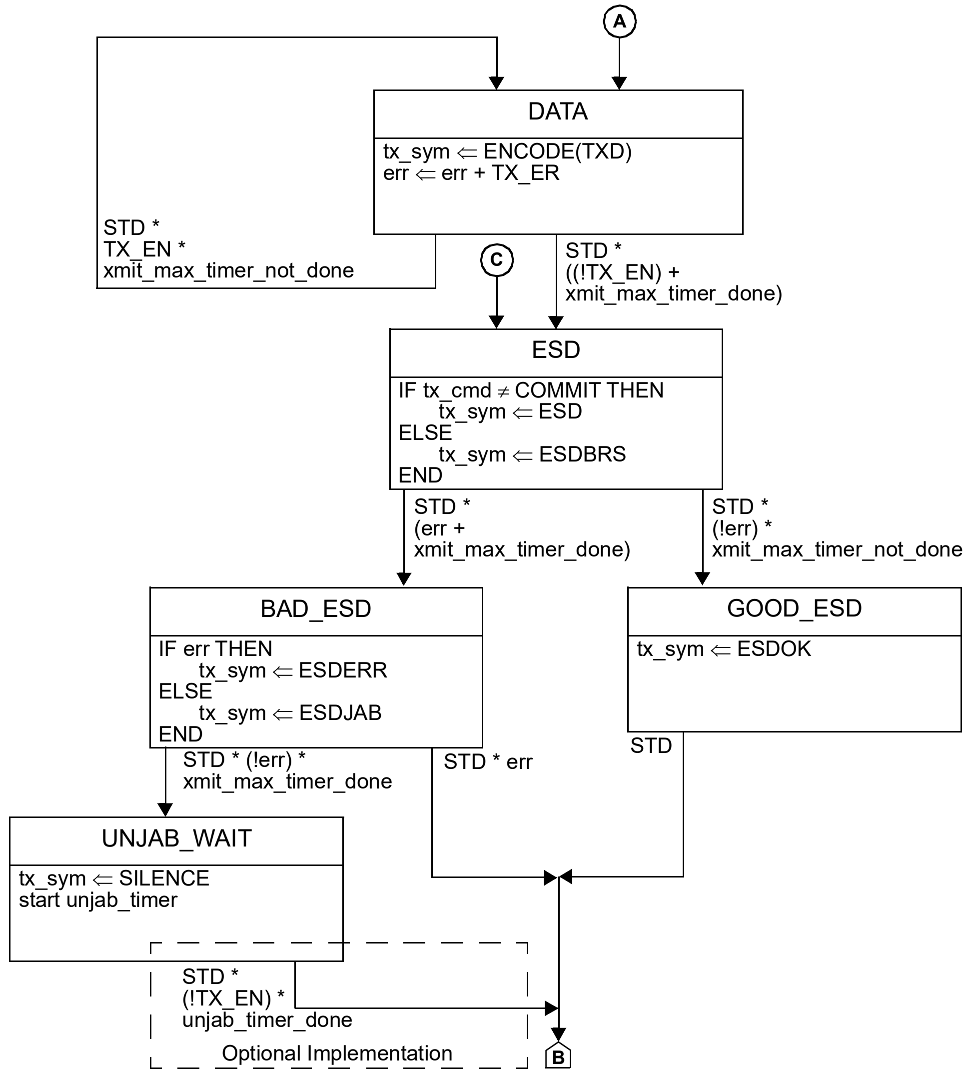


Figure 147–5—PCS Transmit state diagram, part b

147.3.2.8 Self-synchronizing scrambler

The PCS Transmit function shall implement multiplicative scrambling using the following generator polynomial $g(x) = x^{17} + x^{14} + 1$.

An implementation of a self-synchronizing scrambler by a linear-feedback shift register is shown in Figure 147–6. The bits stored in the shift register delay line at time n are denoted by Scr_n<16:0>. The '+' symbol denotes the exclusive-OR logical operation. When Sc_n<3:0> is presented at the input of the scrambler, Sd_n<3:0> is produced by shifting in each bit of Sc_n<3:0> as Sc_n<i>, with i ranging from 0 to 3 (i.e., LSB first). The scrambler is reset upon execution of the PCS Reset function. If the PCS Reset is executed, all bits of the 17-bit vector representing the self-synchronizing scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros. At every STD, if no data is presented at the scrambler input via Sc_n<3:0>, the scrambler may be fed with arbitrary inputs.

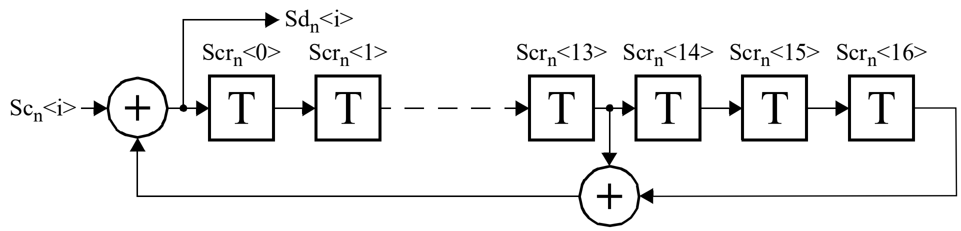


Figure 147–6—Self-synchronizing scrambler

147.3.2.9 Jabber functional requirements

The PCS Transmit function contains the capability to interrupt a transmission that exceeds a time duration determined by xmit_max_timer. If the packet being transmitted continues longer than the specified time duration, the PCS Transmit sends an ESD, ESDJAB symbol sequence to notify the receivers, then it inhibits further transmissions for at least the duration of unjab_timer. The PCS Transmit may return to normal operation automatically after unjab_timer elapsed and the error condition has been cleared, or it may keep silent until reset.

147.3.3 PCS Receive

147.3.3.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 147–7 and Figure 147–8, and associated state variables.

The state diagram defined in Figure 147–7 is triggered by the reception of a SYNC symbol from the PMA Receive function and waits for two SSD symbols to start regenerating the packet preamble whose start has been replaced with the SYNC, SYNC, SSD, SSD sequence by the PCS Transmit function as described in Figure 147–4. After the second SSD is received, the PCS Receive function discards the next nine symbols. These symbols can be used to achieve lock of the self-synchronizing descrambler.

During the descrambler locking time, the special value 5 is conveyed to the MII via the RXD variable in order to rebuild the original preamble transmitted by the MAC.

The DATA state, in which 5B symbols are decoded into MII data, is left when ESD or ESDBRS followed by either ESDOK, ESDERR, or ESDJAB symbol is encountered, or when the PMA detects SILENCE on the media (e.g., the transmitter prematurely stops data transmission).

During the WAIT_SYNC state, the PCS notifies the RS of a received BEACON indication by the means of the MII as specified in 22.2.2.8. When a sequence of at least two consecutive 'N' symbols is received, the MII signals RX_DV, RX_ER, and RXD<3:0> are set to the BEACON indication as shown in Table 22–2. Additionally, the PCS notifies the RS of a received COMMIT indication by the means of the MII as specified in 22.2.2.8. When a sequence of at least two consecutive SYNC is received, the MII signals RX_DV, RX_ER, and RXD<3:0> are set to the COMMIT indication as shown in Table 22–2.

147.3.3.2 Variables

duplex_mode

This variable indicates whether the PHY is configured for full-duplex operation (DUPLEX_FULL) or half-duplex operation (DUPLEX_HALF). If Multidrop mode MDIO register bit 1.2297.10 is set to one and multidrop mode is supported according to bit 1.2298.10 then duplex_mode is set to DUPLEX_HALF. Else, if Auto-Negotiation is enabled then duplex_mode is set by the priority resolution defined in 98B.4. Otherwise, this variable is set by MDIO register bit 3.2291.8. If MDIO is not implemented, duplex_mode is set by equivalent means.
Values: DUPLEX_FULL or DUPLEX_HALF

link_control

See 147.3.2.2.

multidrop

See 147.3.7.1.1.

precnt

Counter for preamble regeneration.

rx_cmd

See 147.3.7.1.1.

RX_DV

The RX_DV signal of the MII as specified in 22.2.2.7.

RX_ER

The RX_ER signal of the MII as specified in 22.2.2.10.

RXD

PCS decoded data synchronous to RX_CLK as specified in 22.2.2.8.

pcs_reset

See 147.3.2.2.

RXn

The rx_sym parameter of the PMA_UNITADATA.indication primitive defined in 147.2.1.
The 'n' subscript denotes the rx_sym conveyed in the most recent recv_symb_conv_timer cycle.
The 'n-x' subscript indicates the rx_sym conveyed 'x' cycles before the most recent one.

transmitting

See 147.3.2.2.

147.3.3.3 Constants

fc_supported

Indicates whether the optional False Carrier detection is supported.
Values: TRUE or FALSE

BEACON

5B symbol defined as 'N' in 4B/5B encoding.

HB

5B symbol defined as 'T' in 4B/5B encoding.

See also 147.3.2.3.

147.3.3.4 Functions

DECODE

This function takes a 5B symbol input parameter and returns a 4 bit value Dc_n<3:0> value according to the following procedure:

1. Convert the 5B input symbol into Dr_n<3:0> by performing a reverse lookup in Table 147–1. If no 4B value is associated to the given 5B symbol, the PCS Receive function shall assert RX_ER for at least one symbol period and Dr_n<3:0> may be set arbitrarily.
2. Convert Dr_n<3:0> to Dc_n<3:0> as specified in 147.3.3.8.

147.3.3.5 Abbreviations

RSCD — Alias for recv_symb_conv_timer_done.

147.3.3.6 Timers

recv_symb_conv_timer

A continuous timer which expires when the PMA_UNITDATA.indication message is generated (see 147.2.1).
Continuous timer: The condition recv_symb_conv_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration.
Duration: timed by the PMA_UNITDATA.indication message generation.

147.3.3.7 State diagrams

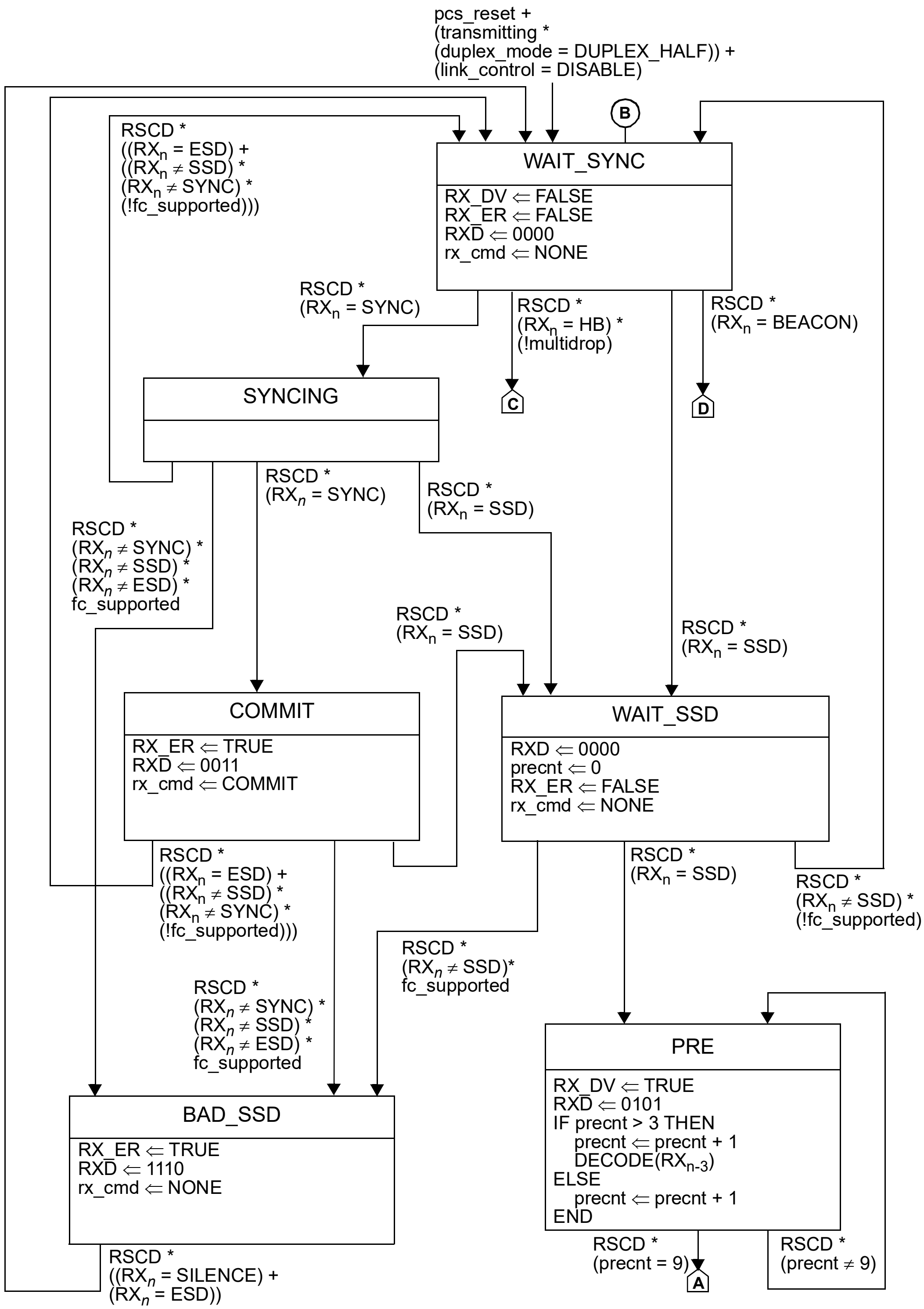


Figure 147–7—PCS Receive state diagram, part a

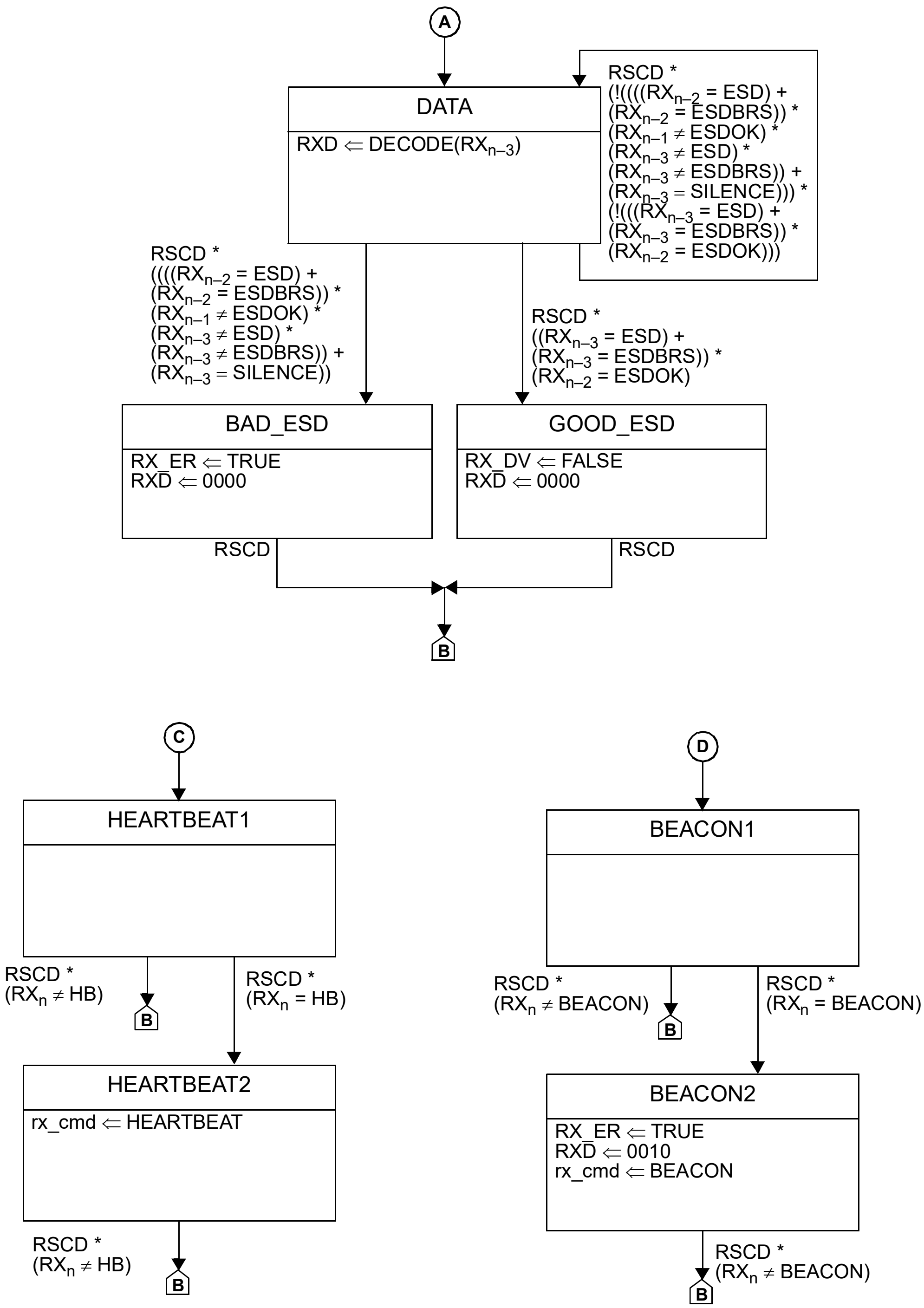


Figure 147–8—PCS Receive state diagram, part b

147.3.3.8 Self-synchronizing descrambler

The PCS Receive function descrambles the 5B/4B decoded data stream and returns the value of RXD<3:0> to the MII. The descrambler shall employ the polynomial $g(x)$ defined in 147.3.2.8. The implementation of the self-synchronizing descrambler by linear-feedback shift register is shown in Figure 147–9. The bits stored in the shift register delay line at time n are denoted by Dcr_n<16:0>. The '+' symbol denotes the exclusive-OR logical operation.

When Dr_n<3:0> is presented at the input of the descrambler, Dc_n<3:0> is produced by shifting in each bit of Dr_n<3:0> as Dr_n<i>, with i ranging from 0 to 3 (i.e., LSB first). The descrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all the bits of the 17-bit vector representing the self-synchronizing descrambler state are arbitrarily set. The initialization of the descrambler state is left to the implementer. At every RSCD, if no data is presented at the descrambler input via Dr_n<3:0>, the descrambler may be fed with arbitrary inputs.

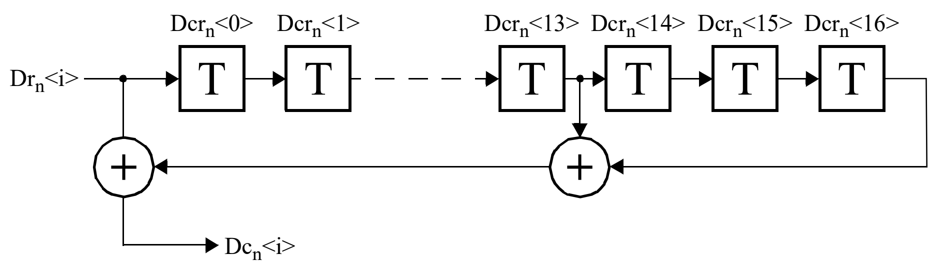


Figure 147–9—Self-synchronizing descrambler

147.3.3.9 Jabber diagnostics

The ESDJAB symbol informs the PCS Receiver that a frame was terminated by the jabber function. The number of received ESDJAB events can be reported to the management entity be the means of MDIO register 3.2293 or similar functionality if MDIO is not implemented.

147.3.4 PCS loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.

147.3.5 Collision detection

When operating in half-duplex mode, the 10BASE-T1S PHY shall detect when a transmission initiated locally results in a corrupted signal at the MDI as a collision. When collisions are detected, the PHY shall assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE.

The method for detecting a collision is implementation dependent but the following requirements have to be fulfilled:

a) The PHY shall assert COL when it is transmitting, and one or more other stations are also transmitting at the same time.
b) The PHY shall assert CRS in the presence of a signal resulting from a collision between two or more other stations.

147.3.6 Carrier sense

When operating in half-duplex mode, the 10BASE-T1S PHY senses when the media is busy and conveys this information to the MAC by asserting the signal CRS on the MII as specified in 22.2.2.11.

CRS is generated by mapping the PMA_CARRIER.indication (pma_crs) primitive to the MII signal CRS:

a) CRS shall be asserted when the pma_crs parameter is CARRIER_ON.
b) CRS shall be deasserted when the pma_crs parameter is CARRIER_OFF.

147.3.7 Support for PCS status generation

If Clause 98 Auto-Negotiation functions are implemented and enabled, the PCS shall conform to the Heartbeat (HB) transmit and receive state diagrams in Figure 147–10, Figure 147–11, and the associated state variables, functions, timers, messages, and constants.

If Clause 98 Auto-Negotiation functions are not implemented or disabled, the PCS_STATUS.indication primitive conveys NOT_OK.

The pcs_status parameter of PCS_STATUS.indication primitive is set to OK after the reception of HB signals or valid data reception (RX_DV) according to the logic described in the HB receive state diagram.

The HB generation is disabled when the PHY is configured for operation over a mixing segment or a BEACON is detected.

147.3.7.1 Heartbeat transmit overview

HB signals are sent unsolicited by the PHY that negotiated the master role during auto-negotiation, while the slave PHY replies back to received HB signals.

A heartbeat is sent only when the PHY is not in the multidrop mode and Auto-Negotiation has completed. The state diagram in Figure 147–10 is held in the INIT state when in the multidrop mode, Auto-Negotiation is not enabled, or Auto-Negotiation signals link_control = DISABLE.

When the PHY is not in multidrop mode and a BEACON request is received from the MII (see Table 22–2) or a BEACON signal is received from the line (see Table 147–1), the state diagram in Figure 147–10 enters the DISABLE_HB state. It remains in the DISABLE_HB state until at least one of the following occurs: PCS Reset is asserted, multidrop mode is enabled, the disable_hb_timer expires, Auto-Negotiation is disabled, or Auto-Negotiation stops reporting that it is complete.

NOTE—Any BEACON received either from the MII or the PMA restarts the disable_hb_timer.

147.3.7.1.1 Variables

pcs_reset
: See 147.3.2.2.

mr_autoneg_enable
: See 98.5.1.

link_control
: See 147.3.2.2.

multidrop
: If MDIO is implemented, this variable is set according to bit 1.2297.10.
If MDIO is not implemented, multidrop should be set by equivalent means.
Values: TRUE or FALSE

master
: Result of the role negotiated using method in 98.2.1.2.5 and Table 98-4.
Values: TRUE (negotiated role is master) or FALSE (negotiated role is slave)

hb_cmd
: Enumerated variable that conveys the command to send an HB message to the PCS transmit function. This command is ignored or interrupted by the PCS transmit function when normal data is being sent or a higher priority request is in effect, as specified in 147.3.2.4.
Values: HEARTBEAT or NONE

rx_cmd
: PLCA or HEARTBEAT signaling decoded by the PCS.

tx_cmd
: See 147.3.2.2.

COL
: The MII signal COL.
Values: TRUE or FALSE

CRS
: The MII signal CRS.
Values: TRUE or FALSE

RX_DV
: The MII signal RX_DV.
Values: TRUE or FALSE

147.3.7.1.2 Timers

disable_hb_timer
: Time the heartbeat state diagram dwells in the DISABLE_HB state without receiving or transmitting a BEACON.
Duration: 1 s
Tolerance: ± 100 ms

hb_send_timer
: Times the duration of the HB signal on the line.
Duration: 20 bit times
Tolerance: ± 0.5 bit times

hb_timer
: Period between the transmission of two consecutive HB signals.
Duration: 50 ms
Tolerance: ± 100 µs

147.3.7.1.3 State diagram

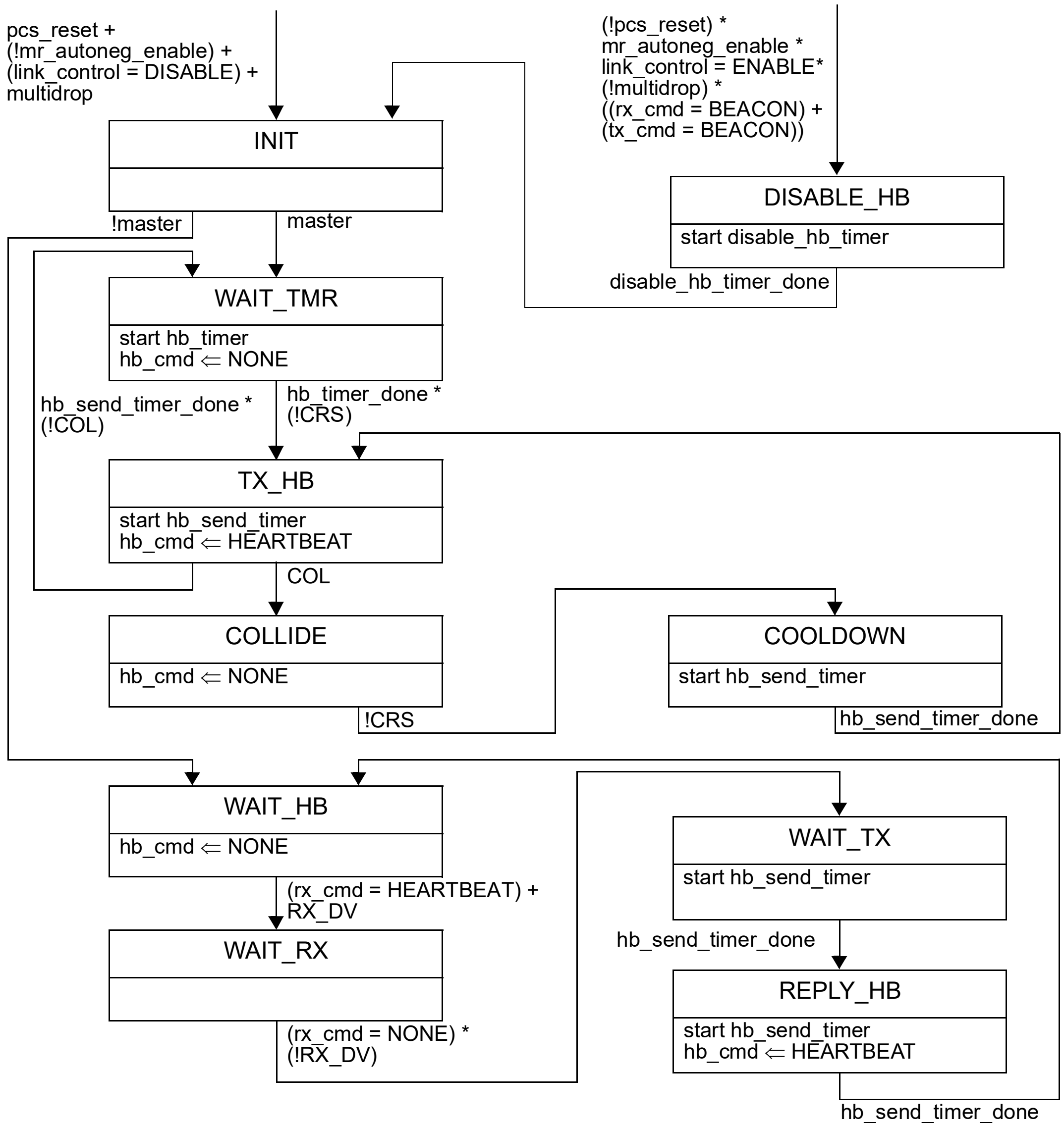


Figure 147–10—Heartbeat transmit state diagram

147.3.7.2 Heartbeat receive overview

The HB receive state diagram in Figure 147–11 generates the pcs_status parameter of the PCS_STATUS.indication primitive based on the reception of valid data packets and HB signals from the remote PHY.

The pcs_status is reported as OK when at least ACTIVE_CNT valid packets or HB messages, separated at max by link_hold_timer ms, are received.

The pcs_status is reported as NOT_OK when PCS is reset or when no valid packets nor HB messages are received within link_hold_timer for INACTIVE_CNT times in a row.

147.3.7.2.1 Variables

pcs_reset
: See 147.3.2.2.

pcs_status
: Parameter of the PCS_STATUS.indication primitive.
Values: OK or NOT_OK

mr_autoneg_enable
: See 98.5.1.

link_control
: See 147.3.2.2.

multidrop
: See 147.3.7.1.1.

rx_cmd
: See 147.3.7.1.1.

cnt_l
: Count of link_hold_timer expiration periods without HBs or receive packet when pcs_status is OK.
Values: integer number between 0 and INACTIVE_CNT

cnt_h
: Counter of HBs and receive packets when pcs_status is NOT_OK.
Values: integer number between 0 and ACTIVE_CNT

COL
: The MII signal COL.
Values: TRUE or FALSE

CRS
: The MII signal CRS.
Values: TRUE or FALSE

RX_DV
: The MII signal RX_DV.
Values: TRUE or FALSE

147.3.7.2.2 Constants

ACTIVE_CNT

Number of combined HBs and receive packets required to signal pcs_status = OK.
Value: integer number between 0 and 7
Default value: 2

INACTIVE_CNT

Number of link_hold_timer expirations without HBs or receive packets required to signal pcs_status = NOT_OK.
Value: integer number between 0 and 7
Default value: 5

147.3.7.2.3 Timers

link_hold_timer

Timer used to check inactivity.
Duration: 75 ms
Tolerance: ± 100 μs

147.3.7.2.4 State diagram

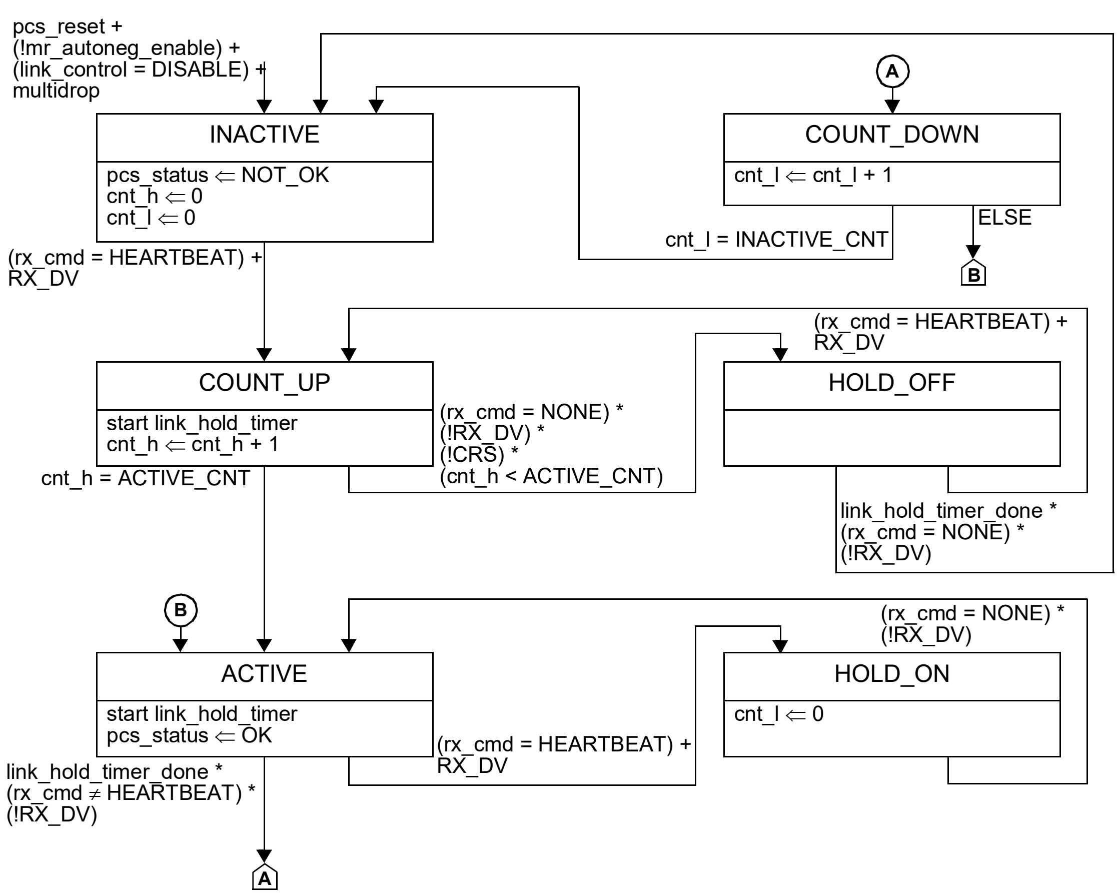


Figure 147–11—Heartbeat receive state diagram

147.4 Physical Medium Attachment (PMA) sublayer

PMA functions are illustrated in Figure 147–12.

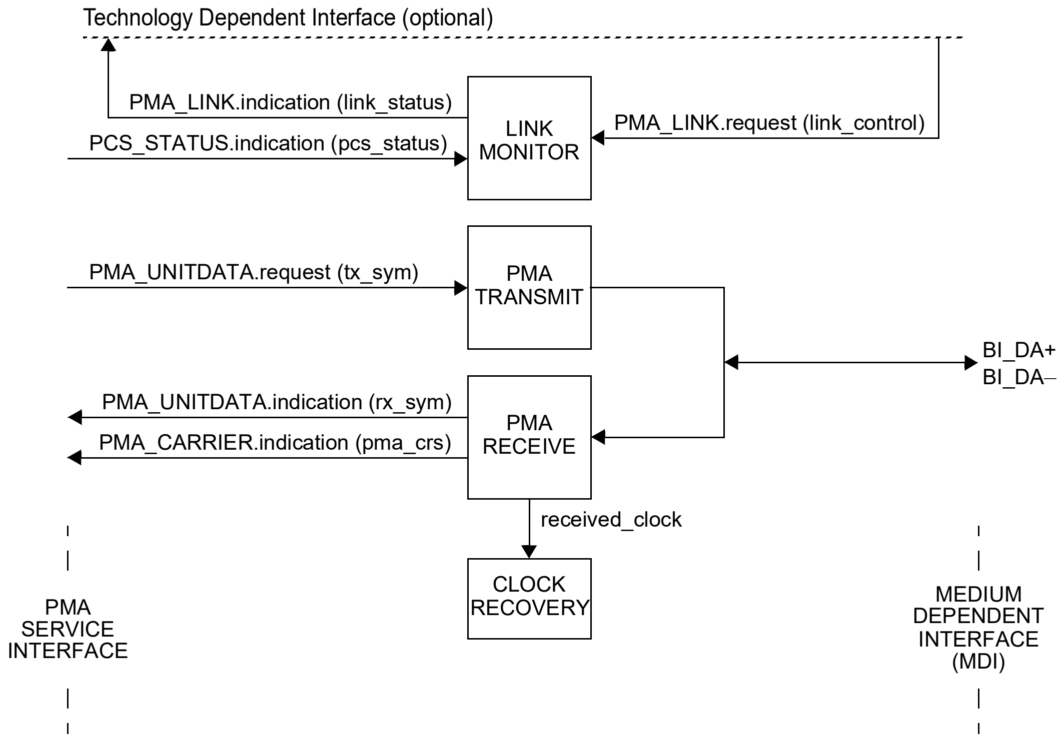


Figure 147–12—PMA functional block diagram

The reference diagrams do not explicitly show the PMA Reset function.

The PMA couples messages from the PMA service interface specified in 147.3.1 onto the 10BASE-T1S physical medium. The PMA provides half duplex communications to and from the medium. Optionally, the PMA may also provide full duplex communications to and from the medium. The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 147.9.

147.4.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

— Power on (see 36.2.5.1.3).
— The receipt of a request for reset from the management entity.

The PMA Reset function carries out the following tasks:

— PMA Transmit output is set to high-impedance state.
— PMA_UNITDATA.indication is cleared.

147.4.2 PMA Transmit function

During transmission, PMA_UNITDATA.request conveys the tx_sym variable to the PMA. The value of the tx_sym variable is sent over the single balanced pair of conductors, BI_DA.

The tx_sym variable is a 5B symbol, to be encoded LSB first, using DME rules defined below:

If the tx_sym parameter value is the special 5B symbol 'I', the PMA shall, in the following order:

a) Transmit an additional DME encoded 0 if the previous value of the tx_sym parameter was anything but the 5B symbol 'I'.
b) When operating in multidrop mode, present the minimum impedance described in 147.9.2 at the MDI. This shall happen within 40 ns after the additional DME encoded 0 has been transmitted.
c) When operating in point-to-point mode, drive BI_DA+ and BI_DA– to the same voltage with 100 Ω nominal impedance, so that their difference is 0 V.

If tx_sym value is anything other than 'I', the following rules apply:

— A "clock transition" shall always be generated at the start of each bit.
— A "data transition" in the middle of a nominal bit period shall be generated if the bit to be transmitted is a logical '1'. Otherwise, no transition shall be generated until the next bit.

See Figure 147–13 and Table 147–2.

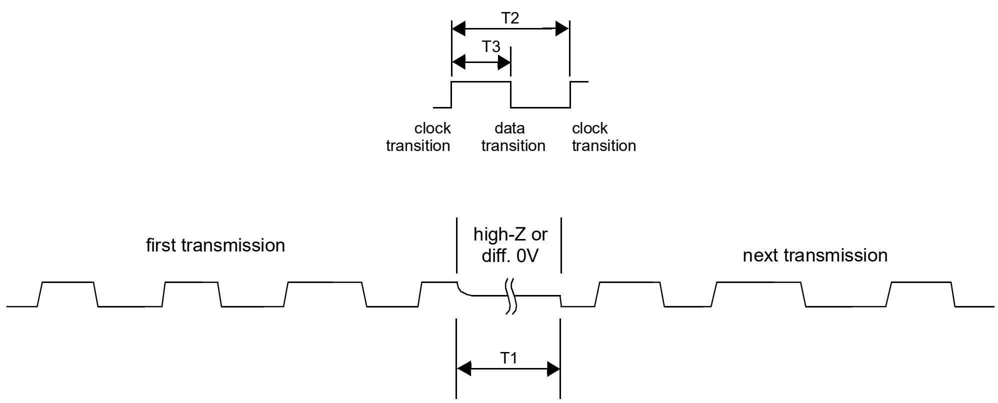


Figure 147–13—DME encoding scheme

Table 147–2—DME timings

Parameter name	Description	Minimum value	Nominal value	Maximum value	Unit of measure
T1	Delay between transmissions	480	—	—	ns
T2	Clock transition to clock transition	–100 ppm	80	+100 ppm	ns
T3	Clock transition to data transition (data = 1)	38	40	42	ns

147.4.3 PMA Receive function

The 10BASE-T1S PMA Receive function comprises a single receiver (PMA Receive) for DME modulated signals on a single balanced pair of conductors, BI_DA. PMA Receive has the ability to translate the received signals on the single balanced pair of conductors into the PMA_UNITDATA.indication parameter rx_sym. It detects 5B symbols from the signals received at the MDI and presents these sequences to the PCS Receive function.

The PMA Receive function recovers encoded clock and data information from the DME encoded stream received at the MDI. The clock recovery provides a synchronous clock for sampling the signal on the pair. While it may not drive the MII directly, the clock recovery function is the underlying source of RX_CLK. In order to meet the specifications of 147.5.5.1, the PMA Receive function must achieve proper synchronization on both the DME stream and the 5B boundary within 800 ns.

The PMA Receive function interprets the signals at the MDI using the inverse mapping described in 147.4.2 for the PMA Transmit function and transfers the 5B code groups by the means of the PMA_UNITDATA.indication. When the PMA Receive function does not detect activity on the line, it shall convey the symbol 'I' (meaning SILENCE).

147.4.4 Link Monitor function

The PMA shall conform to the Link Monitor state diagram in Figure 147–14 and associated variables.

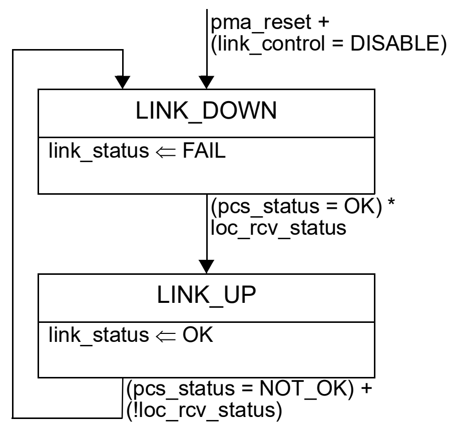


Figure 147–14—Link Monitor state diagram

147.4.4.1 Link Monitor overview

The link monitor function generates the link_status parameter of the PMA_LINK.indication primitive for the Clause 98 Auto-Negotiation function.

The link_status parameter is set after the result of the PCS_STATUS.indication primitive and the implementation defined variable loc_rcv_status.

147.4.4.2 Variables

pma_reset

Allows reset of all PMA functions.
Values: TRUE or FALSE
Set by: PMA Reset function.

link_control

See 147.3.2.2.

loc_rcv_status

Implementation defined variable set to TRUE when the PMA is ready to decode valid data from the line, FALSE otherwise.
Values: TRUE or FALSE

link_status
: The link_status parameter set by PMA Link Monitor and communicated to the Technology Dependent Interface through the PMA_LINK.indication primitive.
Values: OK or FAIL

pcs_status
: See 147.3.7.2.1.

147.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1S PHY.

147.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 147.5.1.1 and 147.5.1.2 may be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements. Operational requirements of the transceiver during the test are determined by the manufacturer.

Applications for the specified device commonly have additional requirements that limit its conducted radio frequency emission and its susceptibility to electromagnetic interference. Such requirements are beyond the scope of this standard.

147.5.1.1 Immunity—DPI test

In a real application radio frequency (RF) common mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of IEC 62132-4.

147.5.1.2 Emission—Conducted emission test

The emission of the PMA transmitter to its electrical environment may be tested according to the 150 Ω direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements.

147.5.2 Test modes

The test modes described in this subclause shall be provided to allow testing of the transmitter. The test modes can be enabled by setting bits 1.2299.15:13 (10BASE-T1S test mode control register) of the PHY Management register set as described in 45.2.1.186f.1. If MDIO is not implemented a similar functionality shall be provided by equivalent means. These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1—Transmitter output voltage, timing jitter
b) Test mode 2—Transmitter output droop test mode
c) Test mode 3—Transmitter PSD mask
d) Test mode 4—Transmitter high impedance mode

When test mode 1 is enabled, the PHY shall repeatedly transmit DME encoded ones.

When test mode 2 is enabled, the PHY shall transmit a positive differential voltage for 1.6 μs followed by a negative differential voltage level for 1.6 μs. This sequence is repeated continually.

When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of positive and negative voltage levels, generated by the scrambler defined in 147.3.2.8 and encoded using DME as in 147.4.2.

PHYs supporting multidrop mode shall implement test mode 4. When test mode 4 is enabled and the PHY is configured for multidrop mode, the transmitter shall present a high impedance termination to the line as specified in 147.4.2 for the 'I' symbol when operating in multidrop mode.

PHYs not supporting multidrop mode are not required to implement test mode 4. When test mode 4 is enabled and the PHY is not configured for multidrop mode, the transmitter behavior is undefined and left up to the implementer.

147.5.3 Test fixtures

The following fixtures (illustrated by Figure 147–15 and Figure 147–16), or their functional equivalents, can be used for measuring the transmitter specifications described in 147.5.4.

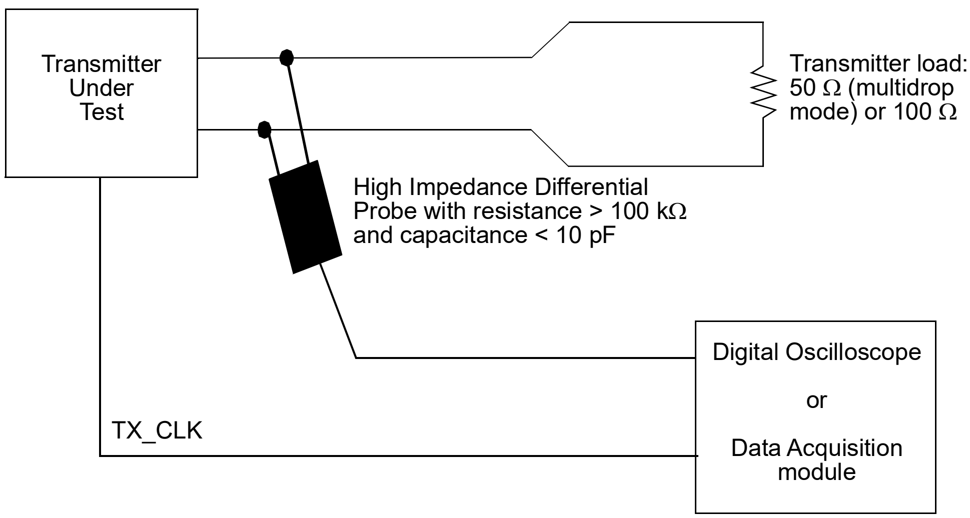


Figure 147–15—Transmitter test fixture 1 for transmitter voltage, transmitter droop, and transmitter timing jitter

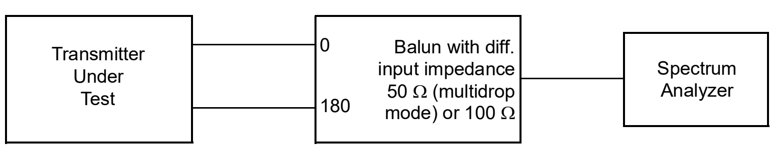


Figure 147–16—Transmitter test fixture 2 for power spectral density (PSD) measurement

To allow an easy synchronization of the measurement equipment, the PHY shall provide access to TX_CLK.

147.5.4 Transmitter electrical specification

The PMA shall operate with AC coupling to the MDI.

Where a load is not specified and multidrop mode is supported and enabled, the transmitter shall meet the requirements of this subclause with a 50 Ω resistive differential load connected to the transmitter output. Otherwise, the transmitter shall meet the requirements of this subclause with a 100 Ω resistive differential load connected to the transmitter output. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

Unless otherwise specified, the specifications in 147.5.4.1 through 147.5.4.5 apply to transmitters in both point-to-point and multidrop mode, if supported.

147.5.4.1 Transmitter output voltage

When tested using the test fixture shown in Figure 147–15 with the transmitter in test mode 1, the transmitter output voltage shall be 1 V ± 20% peak-to-peak differential.

147.5.4.2 Transmitter output droop

When tested using the text fixture shown in Figure 147–15 with the transmitter in test mode 2, the magnitude of both the positive and negative droop measured with respect to the initial peak value after the zero crossing and the value 800 ns after the initial peak, depicted by Figure 147–17, shall be less than 30%.

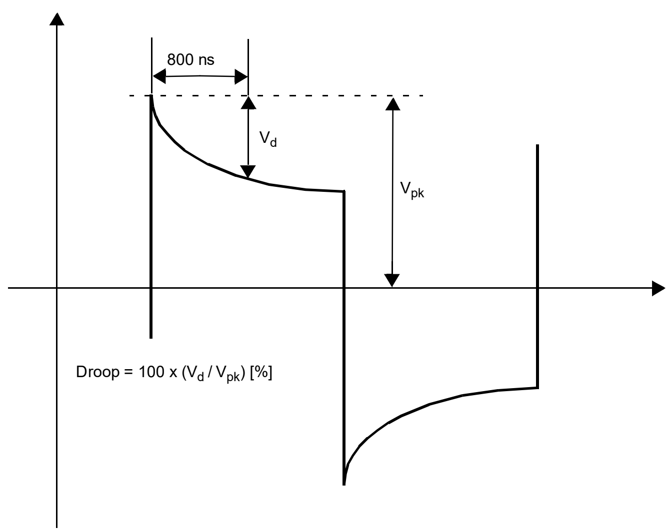


Figure 147–17—Transmitter output droop

147.5.4.3 Transmitter timing jitter

When measured using the test fixture shown in Figure 147–15 with the transmitter in test mode 1, the maximum jitter at the transmitter side shall be less than 5 ns symbol-to-symbol.

147.5.4.4 Transmitter Power Spectral Density (PSD)

When measured using test mode 3 and the test fixture shown in Figure 147–16, or equivalent, the transmitter Power Spectral Density (PSD) shall be between the upper and lower masks specified in Equation (147–1) and Equation (147–2).

The upper and lower limits for multidrop mode are given in Equation (147–1) and Equation (147–2), and shown in Figure 147–18. In point-to-point mode both upper and lower limits are 3 dB lower than those for multidrop mode.

147.5.4.4.1 Upper PSD

$$\mathrm{UpperPSD}(f) = \left\{ \begin{array}{ll} -61 & 0.3 \le f < 15 \\ -40 - 1.4f & 15 \le f < 25 \\ -75 & 25 \le f \le 40 \end{array} \right\} \text{ dBm/Hz} \qquad (147\text{–}1)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

Lower PSD

$$\mathrm{LowerPSD}(f) = \left\{ \begin{array}{ll} -87 + 2f & 5 \le f < 10 \\ -47 - 2f & 10 \le f \le 15 \end{array} \right\} \text{ dBm/Hz} \qquad (147\text{–}2)$$

where

f is the frequency in MHz; $5 \le f \le 15$

147.5.4.4.2 PSD mask

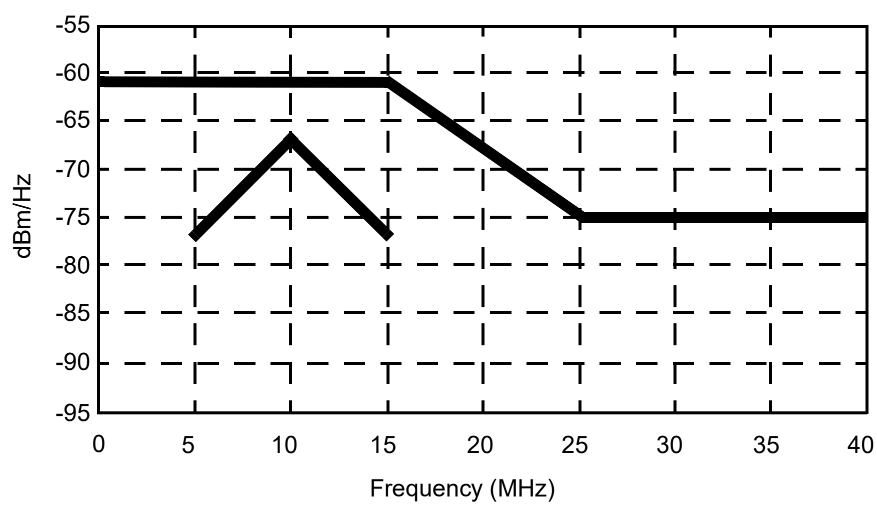


Figure 147–18—PSD upper and lower limits

147.5.4.5 Transmitter high impedance mode

In test mode 4, a transmitter with multidrop mode supported and enabled shall present the minimum parallel impedance across the MDI attachment points as specified in 147.9.2.

147.5.5 Receiver electrical specifications

147.5.5.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 147.5.4 and have passed through a link segment specified in 147.7 or a mixing segment specified in 147.8 shall be received with a Bit Error Ratio (BER) of less than $10^{–10}$, and sent to the MII during normal data transmission. This specification can be verified by a frame error ratio less than $10^{–7}$ for 125 octet frames.

147.5.5.2 Alien crosstalk noise rejection

The test is performed with a noise source such that noise with a Gaussian distribution, bandwidth of 40 MHz, and magnitude of –101 dBm/Hz is present at the MDI.

The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 147–19, with link segments as defined in 147.7 and 147.8. The BER shall be less than $10^{–10}$. This specification may be considered satisfied when the frame loss ratio is less than $10^{–7}$ for 125 octet frames measured at MAC/PLS service interface.

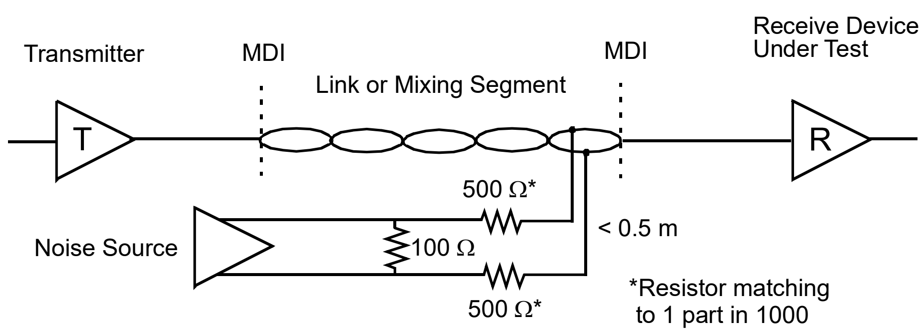


Figure 147–19—Alien crosstalk noise rejection test set-up

147.5.6 PMA local loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or the PMA loopback bit in MDIO register 1.2297.13, defined in 45.2.1.186d.5, is set to one (or PMA loopback mode is enabled by a similar functionality if MDIO is not implemented).

When the PHY is in the PMA local loopback mode, if the PHY supports full-duplex mode of operation, the PMA Receive function utilizes the echo signals from the open MDI and decodes these signals to pass the data back to the MII Receive interface.

If the PHY supports half-duplex mode of operation, the PMA and PCS Receive functions shall pass to the MII RX the data decoded from the signal which is normally received during a transmission for the purpose of detecting collisions.

A MAC client can compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 10BASE-T1S PCS and PMA functions.

147.6 Management interface

10BASE-T1S uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

147.6.1 Support for Auto-Negotiation

Auto-Negotiation may be performed as part of the initial set-up of the link and allows negotiation of the duplex mode of operation. When Auto-Negotiation is used, Technology Ability Field bit A22 contains a one if the PHY is supporting and advertising 10BASE-T1S half duplex ability, and it contains a zero if 10BASE-T1S half duplex communication is not supported or not advertised. When Auto-Negotiation is used, Technology Ability Field bit A1 contains a one if the PHY is supporting and advertising 10BASE-T1S full duplex ability, and it contains a zero if 10BASE-T1S full duplex communication is not supported or not advertised. See 98B.4 for priority resolution.

147.7 Point-to-point link segment characteristics

The transmission characteristics for the 10BASE-T1S point-to-point link segment are specified to support applications requiring short physical reach, such as industrial, automotive, and building automation controls, for up to at least 15 m.

147.7.1 Insertion loss

The insertion loss of each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–3).

$$\text{Insertion loss}(f) < \begin{Bmatrix} 1.0 + \dfrac{1.6(f-1)}{9} & 0.3 \le f < 10 \\ 2.6 + \dfrac{2.3(f-10)}{23} & 10 \le f < 33 \\ 4.9 + \dfrac{2.3(f-33)}{33} & 33 \le f \le 40 \end{Bmatrix} \text{dB} \qquad (147\text{–}3)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

147.7.2 Return loss

In order to limit the noise at the receiver due to impedance mismatches, each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–4) at all frequencies from 0.3 MHz to 40 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return loss}(f) > \begin{Bmatrix} 14 & 0.3 \le f < 10 \\ 14 - 10\log_{10}\left(\dfrac{f}{10}\right) & 10 \le f \le 40 \end{Bmatrix} \text{dB} \qquad (147\text{–}4)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

147.7.3 Mode conversion loss

The mode conversion loss of each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–5).

$$\text{Mode conversion loss}(f) > \left\{ \begin{array}{ll} 43 & 0.3 \le f < 20 \\ 43 - 20\log_{10}\left(\frac{f}{20}\right) & 20 \le f \le 200 \end{array} \right\} \text{ dB} \qquad (147\text{–}5)$$

where

f is the frequency in MHz; $0.3 \le f \le 200$

147.7.4 Power sum alien near-end crosstalk (PSANEXT)

There is no FEXT or NEXT as 10BASE-T1S is a single pair solution. Noise coupled between the disturbed 10BASE-T1S link segment and other disturbing 10BASE-T1S link segments is referred to as alien crosstalk noise. Since the transmitted symbols from the alien noise source in one cable are not available to another cable, cancellation cannot be done. When there are multiple pairs of cables bundled together, where all pairs carry 10 Mb/s links, then each duplex link is disturbed by neighboring links, degrading the signal quality on the victim pair. In order to limit the near-end crosstalk noise for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced), the power sum alien near-end crosstalk (PSANEXT) loss shall meet Equation (147–6).

$$\text{PSANEXT}(f) \ge 31.5 - 10\log_{10}\left(\frac{f}{100}\right) \text{ dB} \qquad (147\text{–}6)$$

where

f is the frequency in MHz; $1 \le f \le 40$

147.7.5 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The power sum alien attenuation to crosstalk ratio far-end (PSAACRF) loss for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced) shall meet Equation (147–7).

$$\text{PSAACRF}(f) \ge 16.5 - 20\log_{10}\left(\frac{f}{100}\right) \text{ dB} \qquad (147\text{–}7)$$

where

f is the frequency in MHz; $1 \le f \le 40$

147.8 Mixing segment characteristics

10BASE-T1S PHYs supporting multidrop mode are designed to operate over media that meet the requirements specified in this subclause. The 10BASE-T1S mixing segment (1.4.331) is a single balanced pair of conductors that may have more than two MDIs attached.

A mixing segment is specified based on cabling that supports up to at least 8 nodes and 25 m in reach. Larger PHY count and/or reach may be achieved provided the mixing segment specifications in 147.8 are met. An example mixing segment and reference points are shown in Figure 147–20.

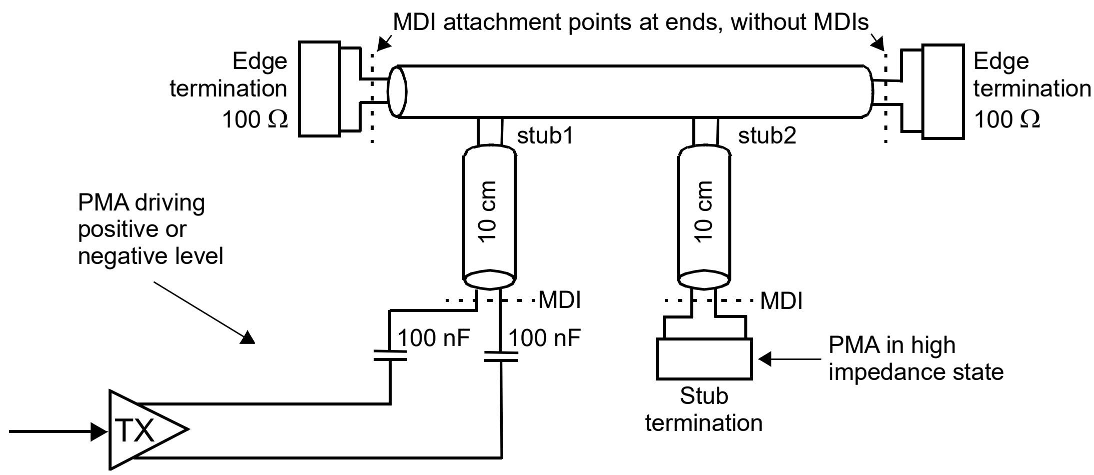


Figure 147–20—Multidrop line termination and PMA

147.8.1 Insertion loss

The mixing segment shall meet the insertion loss characteristics specified for link segments in 147.7.1 between any two MDI attachment points.

147.8.2 Return loss

The mixing segment shall meet the return loss characteristics specified for link segments in 147.7.2 at any MDI attachment point. The reference impedance for the return loss specification is 50 Ω.

147.8.3 Mode conversion loss

The mixing segment shall meet the mode conversion loss characteristics specified for link segments in 147.7.3 between any two MDI attachment points.

147.9 MDI specification

This subclause describes connectors which may be used at the MDI. It also specifies electrical requirements, including fault tolerance, at the MDI.

147.9.1 MDI connectors

In its minimum configuration, the mechanical interface to the balanced cabling is a 3-pin connector (BI_DA+, BI_DA–, and optional SHIELD) or alternatively a 2-pin connector with an optional additional mechanical shield connection which conforms to the link segment specification defined in 147.7 or to the mixing segment specification defined in 147.8.

Specific systems or applications can use connectors or terminals that support the link segment specification defined in 147.7 or the mixing segment specification defined in 147.8.

Connectors meeting the mechanical requirements of IEC 63171-1 [B39a] or IEC 63171-6:2020 [B39b] may be used as the mechanical interface to the balanced cabling. The plug connector is used on the balanced cabling and the MDI jack connector on the PHY. The IEC 63171-1 plug and jack are depicted (for informational use only) in Figure 147–21 and Figure 147–22 respectively, and the mating interface is depicted in Figure 147–23. The IEC 63171-6 plug and jack are depicted (for informational use only) in Figure 147–24 and Figure 147–25 respectively, and the mating interface is depicted in Figure 147–26. These connectors should support link segment DCR characteristics for 1.02 mm (18 AWG) to 0.40 mm (26 AWG) in Table 146B–1.

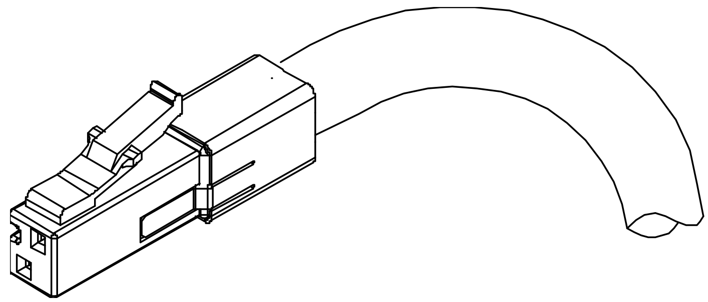


Figure 147–21—IEC 63171-1 plug

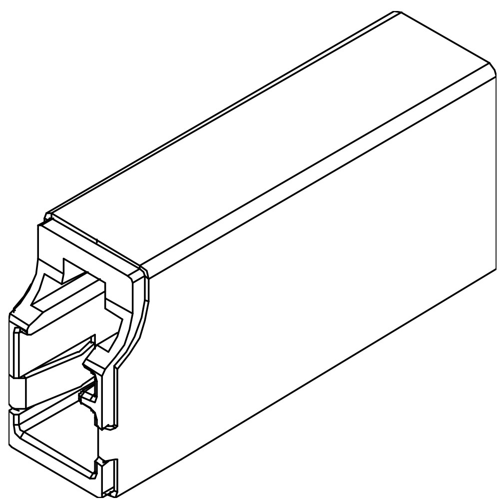


Figure 147–22—IEC 63171-1 jack

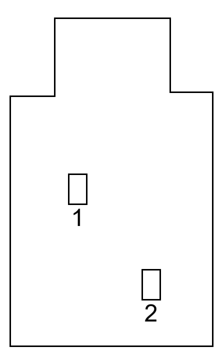


Figure 147–23—IEC 63171-1 mating face

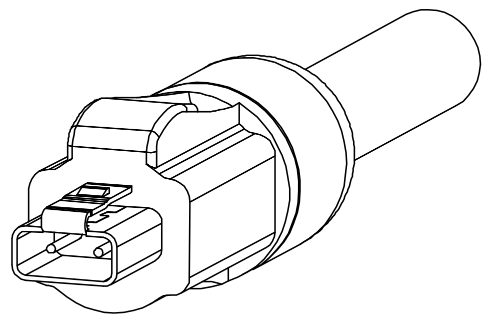


Figure 147–24—IEC 63171-6 plug

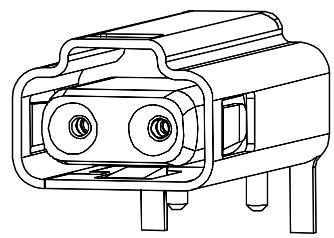


Figure 147–25—IEC 63171-6 jack

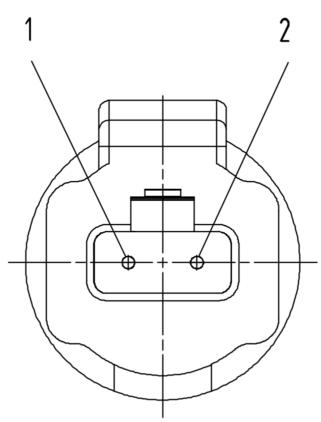


Figure 147–26—IEC 63171-6 mating face

The assignment of PMA signals to connector contacts for PHYs are given in Table 147–3.

Table 147–3—Assignment of PMA signals to MDI contacts

Contact	PMA signal
1	BI_DA+
2	BI_DA–

147.9.2 MDI electrical specification

When not in multidrop mode, the MDI shall meet the return loss limits as specified in Equation (96-12) in 96.8.2.1.

When in multidrop mode, the MDI shall present a minimum parallel impedance across the MDI attachment points per Equation (147–8) and the limits for R, L, C_{tot}, and C_{node} given in Table 147–4 over the stated frequency range. C_{tot} is the maximum total capacitance across all MDI attachment points, while R, L, and C_{node} are the resistance, inductance, and capacitance for each MDI attachment point.

Inductive elements are often used when power is applied across the data lines, and may be absent in non-powered implementations. Removing the parallel inductance is equivalent to setting L to infinity in Equation (147–8). The parasitic capacitance of inductive elements forms a portion of C_{node}.

$$|Z| = \frac{1}{\sqrt{\frac{1}{R^2} + \left(\frac{1}{2\pi \cdot f \cdot L} - 2\pi \cdot f \cdot C_{\mathrm{node}}\right)^2}} \qquad (147–8)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

Table 147–4—MDI impedance limit parameters

Parameter name	Unit of measure	Minimum value	Maximum value
R	kW	10	—
L	μH	80	—
C_{tot}	pF	—	180
C_{node}	pF	—	15

NOTE—The implementer is cautioned that loading the mixing segment with multiple nodes with worst case capacitance at the same location on the mixing segment may cause the mixing segment to exceed its return loss specification.

147.9.3 MDI line powering voltage tolerance

The DTE shall withstand without damage the application of any voltages between 0 V DC and 60 V dc with the source current limited to 2000 mA, applied across BI_DA+ and BI_DA–, in either polarity, under all operating conditions, for an indefinite period of time.

147.9.4 MDI fault tolerance

The wire pair of the MDI shall withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, as per Table 147–5, under all operating conditions indefinitely. Normal operation shall resume after all short circuits have been removed.

Table 147–5—Fault conditions

BI_DA+	BI_DA–
BI_DA–	BI_DA+
Ground	No fault
No fault	Ground
Ground	Ground
+60 V dc	No fault
No fault	+60 V dc
+60 V dc	+60 V dc
Ground	+60 V dc
+60 V dc	Ground

147.10 Environmental specifications

147.10.1 General safety

All equipment subject to this clause is expected to conform to IEC 60950-1, IEC 62368-1, or IEC 61010-1. All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

147.10.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. All 10BASE-T1S cabling is expected to be routed according to any applicable local, state, or national standards considering all relevant safety requirements. In automotive applications, all 10BASE-T1S cabling is expected to be routed to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

147.10.2.1 Environmental safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; this list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

Systems described in this subclause are subject to various environmental hazards during their installation and use. In particular, equipment used in automotive and industrial environments can expect to meet the potential environmental stresses with respect to their mounting location defined for the application. Stresses expected in these environments may include but are not limited to those found in the listed specifications.

The following specifications describe potential environmental stresses in an automotive environment:

- General loads: ISO 16750-1
- Electrical loads: ISO 16750-2, ISO 7637-2, and ISO 8820-1
- Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103-1

— Climatic loads: ISO 16750-4, and IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, IEC 60068-2-64, and IEC 60068-2-78
— Chemical loads: ISO 16750-5 and ISO 20653

The following specifications define potential environmental stresses in an industrial environment:

— Environmental loads: IEC 60529 and ISO 4892
— Mechanical loads: IEC 60068-2-6 and IEC 60068-2-31
— Climatic loads: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-14, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, and IEC 60068-2-78

Additional environment(s) require careful analysis prior to implementation to determine appropriate environmental safety requirements.

147.10.2.2 Electromagnetic compatibility

A system integrating the 10BASE-T1S PHY is expected to comply with all applicable local and national codes for electromagnetic compatibility. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference.

147.11 Delay constraints

The PHY shall comply with the timing requirements specified in Table 147–6.

Table 147–6—10BASE-T1S delay constraints

Event	Minimum value	Maximum value	Unit of measure	Input timing reference	Output timing reference
TX_EN/TX_ER sampled to MDI output	120	440	ns	Rising edge of MII TX_CLK	First DME clock transition at the MDI
MDI input to CRS asserted	400	1040	ns	First DME clock transition at the MDI	Rising edge of CRS
MDI input to CRS deasserted	640	1120	ns	Last DME encoded zero clock transition at the MDI	Falling edge of CRS
MDI input to COL asserted	0	5	µs	Start of corrupted transmitted signal at the MDI	Rising edge of COL
MDI input to COL deasserted	0	3.2	µs	End of transmission at the MDI	Falling edge of COL
MDI input to RX_DV asserted	2.4	4	µs	First DME clock transition at the MDI	Rising edge of RX_DV
MDI input to RX_ER asserted	1.6	4	µs	First DME clock transition at the MDI	Rising edge of RX_ER

147.12 Protocol implementation conformance statement (PICS) proforma for Clause 147, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S[1]

147.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 147, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

147.12.2 Identification

147.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

147.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cg-2019, Clause 147, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cg-2019.)	

Date of Statement	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

147.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MDIO	MDIO Capability	45.1	Register and Interface supported	O	Yes [ ] No [ ]
*HALF	Half-duplex mode			M	Yes [ ] No [ ]
*INS-P2P	Installation / Point-to-point cabling	147.7	Items marked with *INS-P2P include installation practices and cabling specifications for link segments and are not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*INS-MIX	Installation / Mixing segment	147.8	Items marked with *INS-MIX include installation practices and cabling specifications for mixing segments and are not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*MULT	Multidrop mode			O	Yes [ ] No [ ]
MII	PHY associated with MII	147.1.1		O	Yes [ ] No [ ]
PCS	10BASE-T1S PCS	147.3		M	Yes [ ] No [ ]
PMA	10BASE-T1S PMA	147.4		M	Yes [ ] No [ ]
AN	Auto-Negotiation	98		O	Yes [ ] No [ ]
FULL	Full-duplex mode			O	Yes [ ] No [ ]

147.12.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S

147.12.4.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCST1	PCS Reset	147.3.1	See 147.3.1	M	Yes [ ]
PCST2	PCS Data Transmission Enable function	147.3.2.1	Conform to the PCS Transmit state diagram	M	Yes [ ]
PCST3	Values of tx_cmd variable	147.3.2.2	See 147.3.2.2	M	Yes [ ]
PCST4	PCS Transmit function scrambler polynomial	147.3.2.8	$g(x) = x^{17} + x^{14} + 1$	M	Yes [ ]
PCST5	PCS scrambler seed values	147.3.2.8	Never initialized to zeros	M	Yes [ ]
PCST6	xmit_max_timer	147.3.2.6	Upon expiration, an even number of nibbles have been sent	M	Yes [ ]

147.12.4.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PCSR1	PCS Receive function	147.3.3.1	Conform to the PCS Receive state diagram and associated variables	M	Yes [ ]
PCSR2	Generation of RXD<3:0> to the MII	147.3.3.8	Descramble the 5B/4B decoded data stream and return the proper sequence of nibbles	M	Yes [ ]
PCSR3	self-synchronizing descrambler	147.3.3.8	See 147.3.2.8	M	Yes [ ]
PCSR4	False Carrier supported	147.3.3.7	See Figure 147–7	O	Yes [ ]

147.12.4.3 PCS loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCSL1	PCS loopback	147.3.4	The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to one	MDIO: M	Yes [ ] N/A[ ]
PCSL2	PCS loopback function	147.3.4	The PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII	M	Yes [ ]
PCSL3	PHY receive circuitry isolation	147.3.4	The PHY receive circuitry shall be isolated from the network medium	M	Yes [ ]
PCSL4	PHY transmit circuity isolation	147.3.4	The assertion of TX_EN at the MII shall not result in the transmission of data on the network medium	M	Yes [ ]

147.12.4.4 Collision detection

Item	Feature	Subclause	Value/Comment	Status	Support
CD1	Detect collisions on the media during data transmission	147.3.5	When a transmission initiated locally results in a corrupted signal at the MDI, a collision is detected	HALF: M	Yes [ ] N/A[ ]
CD2	When collisions are detected	147.3.5	Assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE	HALF: M	Yes [ ] N/A[ ]
CD3	CRS asserted during collision of two or more other stations	147.3.5	See 147.3.5	HALF: M	Yes [ ] N/A[ ]
CD4	Sense when the media is busy	147.3.6	Assert the signal CRS on the MII as specified in 22.2.2.11	HALF: M	Yes [ ] N/A[ ]

147.12.4.5 Support for PCS status generation

Item	Feature	Subclause	Value/Comment	Status	Support
HB1	Heartbeat behavior when Auto-Negotiation is implemented and enabled	147.3.7	Conforms to Figure 147–10 and Figure 147–11	AN:M	Yes [ ] N/A[ ]

147.12.4.6 Physical Medium Attachment (PMA)

147.12.4.6.1 PMA function

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	PMA reset function	147.4.1	See 147.4.1	M	Yes [ ]
PMA2	tx_sym parameter value is the special 5B symbol 'I'	147.4.2	See 147.4.2	M	Yes [ ]
PMA3	receive SILENCE	147.4.3	PMA receive conveys symbol ‘I’ when no activity is detected on the line.	M	Yes [ ]
PMA4	Link Monitor Function	147.4.4	Conforms to Figure 147–14	M	Yes [ ]

147.12.4.6.2 PMA electrical specification

Item	Feature	Subclause	Value/Comment	Status	Support
PMAE1	Test modes	147.5.2	Implemented in PHY to allow testing transmitter electrical requirements	M	Yes [ ]
PMAE2	Enable test modes	147.5.2	Enable by setting bits 1.2299.15:13 as described in 45.2.1.186f when MDIO implemented; similar functionality provided otherwise	MDIO:M	Yes [ ] N/A[ ]
PMAE3	These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation	147.5.2		M	Yes [ ]
PMAE4	Test mode 1	147.5.2	When enabled, PHY repeatedly transmits DME encoded ones	M	Yes [ ]
PMAE5	Test mode 2	147.5.2	When enabled, PHY repeatedly transmits a positive differential voltage for 1.6 μs followed by a negative differential voltage level for 1.6 μs	M	Yes [ ]
PMAE6	Test mode 3	147.5.2	When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of positive and negative voltage levels, generated by the scrambler defined in 147.3.2.8 and encoded using Differential Manchester Encoding (DME) as in 147.4.2.	M	Yes [ ]
PMAE7	Test mode 4	147.5.2	When enabled, PHY transmitter shall present a high impedance termination to the line as specified in 147.4.2	MULT:M	Yes [ ] N/A[ ]
PMAE8	TX_CLK	147.5.3	PHY to provide access to TX_CLK	M	Yes [ ]
PMAE9	AC coupling at MDI	147.5.4		M	Yes [ ]
PMAE10	The transmitter shall meet the requirements of this subclause with a 100 Ω ± 0.1% resistive differential load connected to the transmitter output	147.5.4		M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PMAE11	The transmitter shall meet the requirements of this subclause with a 50 Ω ± 0.1% resistive differential load connected to the transmitter output when multidrop mode is supported and enabled	147.5.4		MULT:M	Yes [ ] N/A[ ]
PMAE12	Transmitter output voltage	147.5.4.1	1.0 V ± 20% peak-to-peak differential when measured on test mode 1	M	Yes [ ]
PMAE13	Transmitter output droop	147.5.4.2	Less than 30% when measured on test mode 2	M	Yes [ ]
PMAE14	Transmitter timing jitter	147.5.4.3	Less than 5 ns symbol-to-symbol jitter when measured on test mode 1	M	Yes [ ]
PMAE15	Transmit power spectral density	147.5.4.4	Between the upper and lower masks specified in Equation (147–1) and Equation (147–2) when measured on test mode 3	M	Yes [ ]
PMAE16	A transmitter with multidrop mode supported and enabled, and configured for test mode 4	147.5.4.5	Presents the minimum parallel impedance across the MDI attachment points	M	Yes [ ]
PMAE17	Receiver differential input signals	147.5.5.1	Can be verified with a frame error ratio less than 1×10^{-7} for 125 octet frames	M	Yes [ ]
PMAE18	Alien crosstalk noise rejection	147.5.5.2	BER < 10^{-10} with an alien crosstalk noise of Gaussian distribution of magnitude of –101 dBm/Hz and bandwidth of 40 MHz at the MDI	M	Yes [ ]
PMAE19	PMA local loopback	147.5.6	The PMA shall be placed in loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or in MDIO register 1.2297.13, defined in 45.2.1.186d.5 is set to one	MDIO:O	Yes [ ] No [ ] N/A[ ]
PMAE20	PMA local loopback in half-duplex mode	147.5.6	The PMA and PCS Receive functions pass the data decoded from the signal to the MII RX	HALF*MDIO:M	Yes [ ] No [ ] N/A[ ]

147.12.4.7 Point-to-point link Segment characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
PPLS1	Insertion loss	147.7.1	See Equation (147–3)	INS-P2P:M	Yes [ ]
PPLS2	Return loss	147.7.2	See Equation (147–4)	INS-P2P:M	Yes [ ]
PPLS3	Mode conversion loss	147.7.3	See Equation (147–5)	INS-P2P:M	Yes [ ]
PPLS4	Power sum ANEXT loss between a disturbed 10BASE-T1S link segment and the disturbing 10BASE-T1S link segment	147.7.4	Power sum alien near-end crosstalk (PSANEXT) loss shall meet Equation (147–6)	INS-P2P:M	Yes [ ]
PPLS5	Power sum AACRF loss between a disturbed 10BASE-T1S link segment and the disturbing 10BASE-T1S link segment	147.7.5	Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) loss shall meet Equation (147–7)	INS-P2P:M	Yes [ ]

147.12.4.8 Mixing Segment characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
MXS1	Insertion loss	147.8.1	See 147.7.1. Measured between any pair of MDI attachment points	INS-MIX:M	Yes [ ]
MXS2	Return loss	147.8.2	See 147.7.2. Measured with a reference impedance of 50 Ω	INS-MIX:M	Yes [ ]
MXS3	Mode conversion loss	147.8.3	See 147.7.3. Measured between any two MDI attachment points	INS-MIX:M	Yes [ ]

147.12.4.9 MDI specification

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	MDI return loss when not in multidrop mode	147.9.2	Meet Equation (96-12)	M	Yes [ ]
MDI2	Minimum parallel impedance across the MDI attachment points when in multidrop mode	147.9.2	See Equation (147–8)	MULT: M	Yes [ ] N/A[ ]
MDI3	MDI line powering voltage tolerance	147.9.3	Up to 60 V dc with the source current limited to 2000 mA	M	Yes [ ]
MDI4	MDI fault tolerance	147.9.4	Withstand without damage the application of a short circuit of any wire to the other wire of the same pair or ground potential. Normal operation resumes after all short circuits are removed.	M	Yes [ ]

147.12.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Delay constraints	147.11	Comply with Table 147–6	M	Yes [ ]

148. PLCA Reconciliation Sublayer (RS)

148.1 Introduction

This clause specifies a Reconciliation Sublayer to provide optional Physical Layer Collision Avoidance (PLCA) capabilities among participating stations. The PLCA RS is specified for operation with Clause 147 (10BASE-T1S) PHYs operating in half-duplex multidrop mode. PLCA can be dynamically enabled or disabled via management interface. When PLCA is disabled, the Reconciliation Sublayer mapping is identical to that specified in Clause 22.

When enabled, the PLCA RS aligns data from the MAC with transmission opportunities of the Physical Layer and maps the Physical Layer signals to PLS primitives towards the MAC. The use of PLCA-enabled Physical Layers in CSMA/CD half-duplex shared-medium networks can provide enhanced bandwidth and improved access latency under heavily loaded traffic conditions. PLCA-enabled nodes can coexist with nodes without PLCA enabled on the same mixing segment, all using IEEE 802.3 CSMA/CD.

148.1.1 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

148.1.1.1 State diagram notation

The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE, all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE, the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

148.1.1.2 State diagram timer specifications

All timers operate in the manner described in 40.4.5.2.

148.1.1.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

148.2 Overview

The working principle of PLCA is that transmit opportunities on a mixing segment are granted in sequence based on a node ID unique to the local collision domain (set by the management entity). The method of determination of the node ID and to_timer by the management entity is beyond the scope of this standard. Proper operation of the Clause 148 functionality assumes that the assigned node ID is unique in the local collision domain.

The node ID assignment value does not appear externally or in the payload packet format. The node ID assignment value is fully contained within the local collision domain.

Transmit opportunities are generated in a round-robin fashion. The node with ID = 0 signals a BEACON on the medium. Reception of a BEACON indicates the start of a new cycle of transmit opportunities. If the node with ID = 0 fails, the network is still operational with the same performance level of a CSMA/CD network without PLCA.

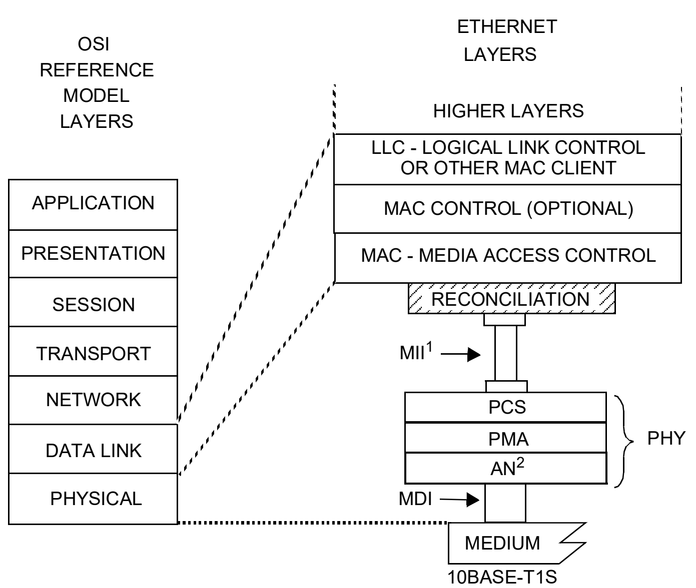
Each node is allowed to transmit a single packet during its own transmit opportunity. Individual nodes can be enabled to transmit a number of additional packets, up to the configured limit, within the same transmit opportunity.

PLCA relies on the PLS_SIGNAL.indication and PLS_CARRIER.indication primitives to have the MAC delay transmission until a transmit opportunity is available.

PLCA-enabled nodes may be used in the same CSMA/CD collision domain as non-PLCA enabled nodes. As the percentage of non-PLCA enabled nodes increases, performance advantages also decrease. If the node with ID = 0 fails, the network is still operational with the same performance level of a CSMA/CD network without PLCA.

148.3 Relationship with other IEEE standards

The relationship between the PLCA Reconciliation Sublayer, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet model is shown in Figure 148–1. The Reconciliation Sublayer (shown shaded) in Figure 148–1 connects one Clause 4 Media Access Control (MAC) layer to the PHY. MII is defined in Clause 22.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

NOTE 1—MII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 148–1—Relationship of PLCA Reconciliation Sublayer to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

148.4 PLCA Reconciliation Sublayer operation

148.4.1 General

This subclause specifies services provided by the PLCA RS as an extension to the RS specified in Clause 22. Figure 148–2 depicts the RS interlayer service interfaces. The PLCA RS contains the Control and Data state diagrams, the variable delay line, and command detect logic. When PLCA functions are not supported or are disabled by the management interface (plca_en = FALSE), RS operation shall conform to the RS definition in Clause 22.

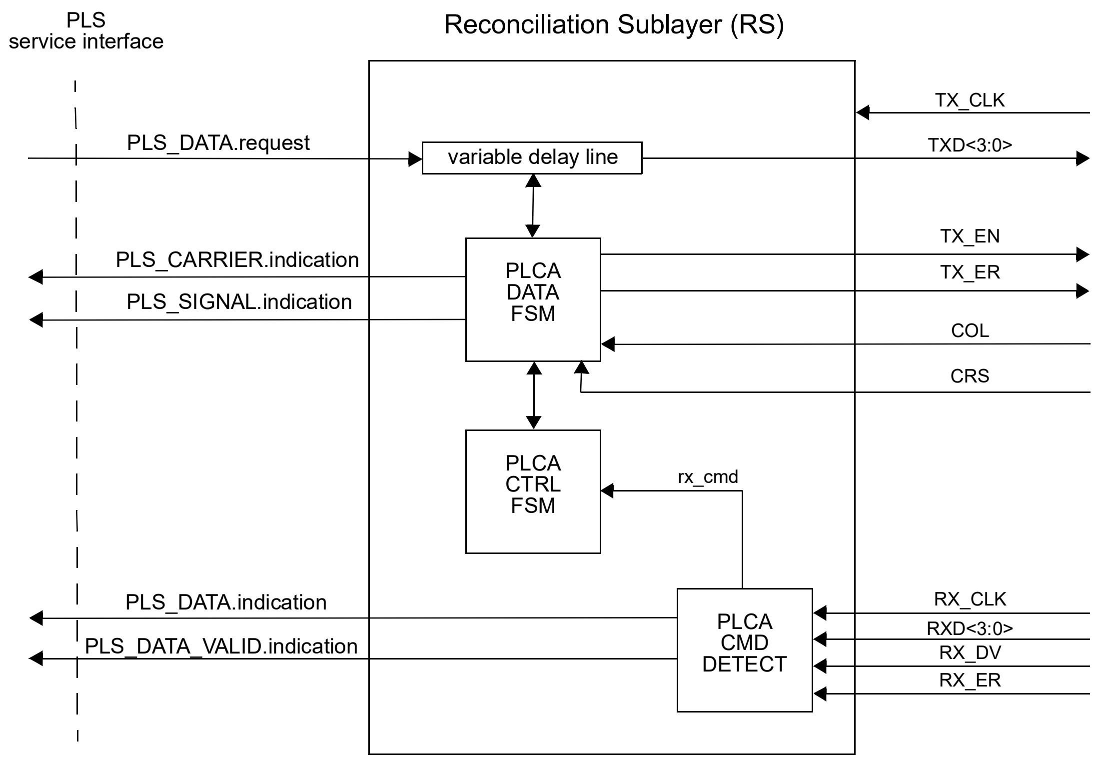


Figure 148–2—PLCA functions within the Reconciliation Sublayer (RS)

148.4.2 Mapping of MII signals to PLS service primitives and PLCA functions

The RS maps the signals provided at the MII to the PLS service primitives defined in Clause 6 via the PLCA state diagrams, variables, and functions (see 148.4.4 and 148.4.5). The PLS service primitives provided by the RS behave in exactly the same manner as defined in Clause 6.

148.4.2.1 Mapping of PLS_DATA.request

When PLCA is disabled (plca_en = FALSE), the mapping of the PLS_DATA.request primitive shall be the one specified in 22.2.1.1. Otherwise, the following applies.

148.4.2.1.1 Function

Maps the primitive PLS_DATA.request to PLCA variables which in turn generate the MII signals TXD<3:0> and TX_EN.

148.4.2.1.2 Semantic of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the individual bits of the four-bit variable plca_txd<3:0>. Each bit of plca_txd<3:0> conveys one bit of data while plca_txen is set to TRUE. The value DATA_COMPLETE is conveyed by setting the variable plca_txen to FALSE. MII signals TXD<3:0> and TX_EN are generated by way of the PLCA Data state diagrams specified in 148.4.5. Synchronization between the RS and the PHY is achieved by way of the TX_CLK signal.

148.4.2.1.3 When generated

The plca_txd<3:0> and plca_txen variables are assigned after every group of four PLS_DATA.request transactions from the MAC sublayer to request the PLCA functions to transmit a nibble of data when the transmit opportunity is available, or to signal the end of the transmission. The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the RS according to PLCA Data state diagrams (see 148.4.5).

148.4.2.2 Mapping of PLS_DATA.indication

Map of the primitive PLS_DATA.indication shall comply with 22.2.1.2.

148.4.2.3 Mapping of PLS_CARRIER.indication

When PLCA is disabled (plca_en = FALSE), the mapping of the PLS_CARRIER.indication primitive shall be the one specified in 22.2.1.3. Otherwise, the following applies

148.4.2.3.1 Function

Maps the primitive PLS_CARRIER.indication to the PLCA Data state diagram.

148.4.2.3.2 Semantic of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF.

148.4.2.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the RS according to the PLCA Data state diagram specified in 148.4.5.

148.4.2.4 Mapping of PLS_SIGNAL.indication

When PLCA is disabled (plca_en = FALSE) the mapping of the PLS_SIGNAL.indication primitive shall be the one specified in 22.2.1.4. Otherwise, the following applies.

148.4.2.4.1 Function

Map the primitive PLS_SIGNAL.indication to the PLCA Data state diagram.

148.4.2.4.2 Semantic of the service primitive

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR.

148.4.2.4.3 When generated

SIGNAL_STATUS is generated by the PLCA Data state diagram specified in 148.4.5.

148.4.2.5 Mapping of PLS_DATA_VALID.indication

Map of the primitive PLS_DATA_VALID.indication shall comply with 22.2.1.7.

148.4.2.6 Generation of TX_ER

Generation of TX_ER shall comply with the PLCA Data state diagram specified in 148.4.5.1.

148.4.2.7 Response to RX_ER indication

Response to RX_ER indication from the MII shall comply with 22.2.1.5.

148.4.3 Requirements for the PHY

In order to support PLCA, the RS has to be connected to a 10BASE-T1S PHY.

148.4.3.1 PHY response to PLCA commands and notifications

148.4.3.1.1 BEACON request

The BEACON function is specified in 148.4.4.1.

The RS conveys the BEACON request via MII interface.

Upon the reception of this request, the PHY encodes and transmits a signal communicating the BEACON to other PHYs on the segment so that they generate a BEACON indication.

Upon the reception of this request, the RX_DV signal is not asserted.

PHYs may map the BEACON request to any suitable line coding as long as the requirements defined in this subclause are met.

148.4.3.1.2 COMMIT request

The COMMIT function is specified in 148.4.4.1.

The PLCA Control state diagram generates a COMMIT request by way of the tx_cmd variable as specified in 148.4.4.2. The RS conveys such request via MII interface as defined in 22.2.2.4.

Upon the reception of this request, the RX_DV signal is not asserted.

PHYs may map the COMMIT request to any suitable line coding as long as the requirement defined in this subclause are met.

148.4.3.2 Mapping of MII signals to PLCA variables

The PLCA RS is required to decode PLCA-specific signaling out of the MII.

148.4.3.2.1 BEACON indication

When the PHY receives a BEACON, it indicates this information to the RS by asserting MII signals.

The RS shall react to such indication by setting the PLCA variable rx_cmd to the value BEACON. The RS shall also reset the rx_cmd variable to NONE when the BEACON indication on the MII ceases, unless a COMMIT indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.2.

148.4.3.2.2 COMMIT indication

When the PHY receives a COMMIT from the line, it indicates this information to the RS by asserting MII signals. The PHY asserts CRS when a COMMIT indication is detected.

The RS shall react to such indication by setting the PLCA variable rx_cmd to the value COMMIT. The RS shall also reset the rx_cmd variable to NONE when the COMMIT indication on the MII ceases, unless a BEACON indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.1.

148.4.4 PLCA Control

148.4.4.1 PLCA Control state diagram

The PLCA Control function shall conform to the PLCA Control state diagram in Figure 148–3 and Figure 148–4 and associated state variables, functions, timers, and messages.

To achieve error free operation the PLCA node should be configured appropriately before transmit functions are enabled. Appropriate configuration includes the following:

a) Each local_nodeID is unique to the local collision domain.
b) There is one and only one node with local_nodeID = 0 on the local collision domain.
c) The transmit opportunity timer (to_timer) is set equal across all the nodes on the local collision domain.
d) plca_node_count is set on the node with local_nodeID = 0 to the maximum number of nodes supported on the local collision domain.

When PLCA functions are enabled and local_nodeID equals zero, PLCA switches to RECOVER state and waits one cycle of transmit opportunities. This prevents sending a BEACON at an inappropriate time (e.g., when the node with local_nodeID = 0 resets in the middle of a cycle of transmit opportunities and other nodes could still be sending valid data). A BEACON is then generated by such node by switching to SEND_BEACON state. On reception of a BEACON, all other nodes reset their own transmit opportunity counter and related timer.

When PLCA functions are enabled, nodes with nonzero local_nodeID wait in RESYNC state until a BEACON is received.

All nodes, including the one generating the BEACON, detect the end of the BEACON condition before proceeding to WAIT_TO state, in order to minimize latency differences across the network.

Entering WAIT_TO state, the node waits for one of these possible conditions:

1) CRS is asserted by the PHY through MII, indicating there is activity on the line.
2) curID becomes equal to local_nodeID while packetPending variable is TRUE, meaning that this node now owns a transmit opportunity and does have a packet to transmit.
3) curID becomes equal to local_nodeID while packetPending variable is FALSE, meaning that this node now owns a transmit opportunity but does not have a packet to transmit.
4) to_timer elapses, indicating the current transmit opportunity is yielded.

If condition (1) occurs, the node is about to receive either a valid packet, a COMMIT request, a BEACON request or it might be receiving a false carrier event.

In EARLY_RECEIVE state, the PLCA Control state diagram is waiting for the PHY to properly decode the incoming signal and to take the following actions:

— Switch to RECEIVE state if a COMMIT indication is reported or a valid packet is being decoded. The PLCA Control state diagram then remains in the RECEIVE state until the line is free (CRS deasserted).
— Switch to RESYNC state if a BEACON is received with local_nodeID ≠ 0, which starts a new cycle of transmit opportunities.
— Switch to RESYNC state if CRS is not followed by the reception of a packet and local_nodeID ≠ 0, meaning that a false carrier occurred and the curID variable might be out of synchronization. In this case, the node skips its transmit opportunity (TO) and waits for a new BEACON in order not to disrupt the current cycle of transmit opportunities.
— Switch to RECOVER state if local_nodeID is 0 and CRS is de-asserted but no packet is being received. In RECOVER state, since the curID variable might be out of synchronization, this node waits for the end of the current cycle of transmit opportunities before sending a new BEACON. This is required so as not to send a BEACON while other nodes might still be using their TO.

When condition (2) occurs, the node now gets a TO having at least one packet to be transmitted. COMMIT state is then entered to signal other nodes to stop their to_timer and wait for a packet by the means of a COMMIT request. COMMIT state is left once the data to be transmitted is available from the MAC or the PLCA delay line.

When condition (3) occurs, the node now gets a TO without being ready to send any packet. In this case, the YIELD state is entered to skip the TO, allowing other nodes a chance to transmit. In some rare cases (e.g., a non-PLCA enabled node is connected to the network) it is possible to receive data in YIELD state. If this unlikely event happens, PLCA switches to RECEIVE state to wait until the end of the transmission and increment curID properly.

When condition (4) is met, another node has yielded its transmit opportunity, causing the curID variable to be incremented and to_timer to be reset.

148.4.4.2 PLCA Control variables

plca_reset

The plca_reset signal is used to reset the optional PLCA function in the RS. This signal maps to TRUE when acPLCAReset is in reset and to FALSE when acPLCAReset is normal, but is further qualified.
Values: TRUE or FALSE

plca_en
: The plca_en signal controls the optional PLCA function in the RS. This signal maps to TRUE when aPLCAAdminState is enabled and to FALSE when aPLCAAdminState is disabled.
Values: TRUE or FALSE

CRS
: The MII signal CRS.
Values: TRUE or FALSE

RX_DV
: The MII signal RX_DV.
Values: TRUE or FALSE

receiving
: Defined as: (RX_DV = TRUE) + (rx_cmd = COMMIT).
Values: TRUE or FALSE

tx_cmd
: Command for the PLCA Data state diagram to convey to the PHY via the MII.
Values: NONE, BEACON or COMMIT

rx_cmd
: Encoding present on RXD<3:0>, RX_ER, and RX_DV as defined in Table 22–2.
Values:
BEACON: PLCA BEACON indication encoding present on RXD<3:0>, RX_ER, and RX_DV
COMMIT: PLCA COMMIT indication encoding present on RXD<3:0>, RX_ER, and RX_DV
NONE: PLCA BEACON or COMMIT indication encoding not present on RXD<3:0>, RX_ER, and RX_DV

TX_EN
: The MII signal TX_EN.
Values: TRUE or FALSE

local_nodeID
: ID representing the PLCA transmit opportunity number assigned to the node. This signal maps to aPLCALocalNodeID.
Values: integer value from 0 to 255

plca_node_count
: Maximum number of PLCA nodes on the mixing segment receiving transmit opportunities before the node with local_nodeID = 0 generates a new BEACON, reflecting the value of aPLCANodeCount. This parameter is meaningful only for the node with local_nodeID = 0; otherwise, it is ignored.
Values: integer number from 0 to 255

committed
: Internal variable used to synchronize PLCA Control and Data functions.
It is set by PLCA Control state diagram to signal that the current transmit opportunity has been committed and the PLCA Data state diagram is now allowed to convey MII data to the PHY.
Values: TRUE or FALSE

packetPending
: Internal variable used to synchronize PLCA Control and Data functions.
The PLCA Data state diagram sets this variable when it detects the MAC is ready to send a packet and have PLCA Control state diagram actually commit for the next available transmit opportunity.
Values: TRUE or FALSE

bc
: Counts the number of additional packets currently sent in a burst after the first transmission.
Values: integer from 0 to 255

max_bc
: Maximum number of additional packets the node is allowed to transmit in a single burst. This signal maps to aPLCAMaxBurstCount attribute.
Values: integer from 0 to 255

plca_active
: Notifies the PLCA Status function whether the node is waiting for sending or receiving a BEACON or it already sent or received one.
Values: TRUE or FALSE

curID
: Integer variable tracking the ID of the node that currently owns a transmit opportunity.
Values: integer from 0 to 255

PMCD
: Prescient mii_clock_done. This variable is set false on entry to the RSYNC state and becomes TRUE 1 ± ½ bit time prior to mii_clock_done becoming TRUE.
Values: TRUE or FALSE

148.4.4.3 Functions

No functions are defined for the PLCA Control state diagram.

148.4.4.4 Timers

beacon_timer
: Times the duration of the BEACON signal.
Duration: 20 bit times.
Tolerance: ± ½ bit time.

beacon_det_timer
: Timer for detecting received BEACONs.
Duration: 22 bit times.
Tolerance: ± 1 bit time.

invalid_beacon_timer
: Timer used for BEACON validation. This timer is stopped any time rx_cmd = BEACON.
Duration: 4000 ns.
Tolerance: ± 400 ns.

burst_timer
: This timer determines how long to wait for the MAC to send a new packet before yielding the transmit opportunity. For PLCA burst mode to work properly this timer should be set greater than one IPG. Timer duration maps to aPLCABurstTimer attribute.
Duration: integer number between 0 and 255, expressed in bit times.
Tolerance: ± ½ bit time.
The default value is specified in 30.16.1.1.7.

to_timer

The transmit opportunity timer maps to aPLCATransmitOpportunityTimer. The timer value needs to meet Equation (148–1). The to_timer should be set equal across the mixing segment for PLCA to work properly.

$$\begin{aligned} to\_timer > {} & 2 \times \max(t_{propdelay}) + \\ & \max(TX\_EN\ sampled\ to\ MDI\ output) + \\ & \max(MDI\ input\ to\ CRS\ asserted) + \\ & \max(MDI\ input\ to\ CRS\ deasserted) - \\ & \min(MDI\ input\ to\ CRS\ deasserted) + \\ & \max(MII\ propagation\ delay) \end{aligned} \quad (148\text{–}1)$$

where $t_{propdelay}$ is the propagation delay between any two nodes on the mixing segment, and the delay specifications are the maxima and minima for the PHY type on the mixing segment (for 10BASE-T1S, see 147.11).

Duration: integer number between 1 and 255, expressed in bit times.
Tolerance: 100 ppm.
The default value is specified in 30.16.1.1.5.

148.4.4.5 Abbreviations

MCD See 148.4.5.5

148.4.4.6 State diagram

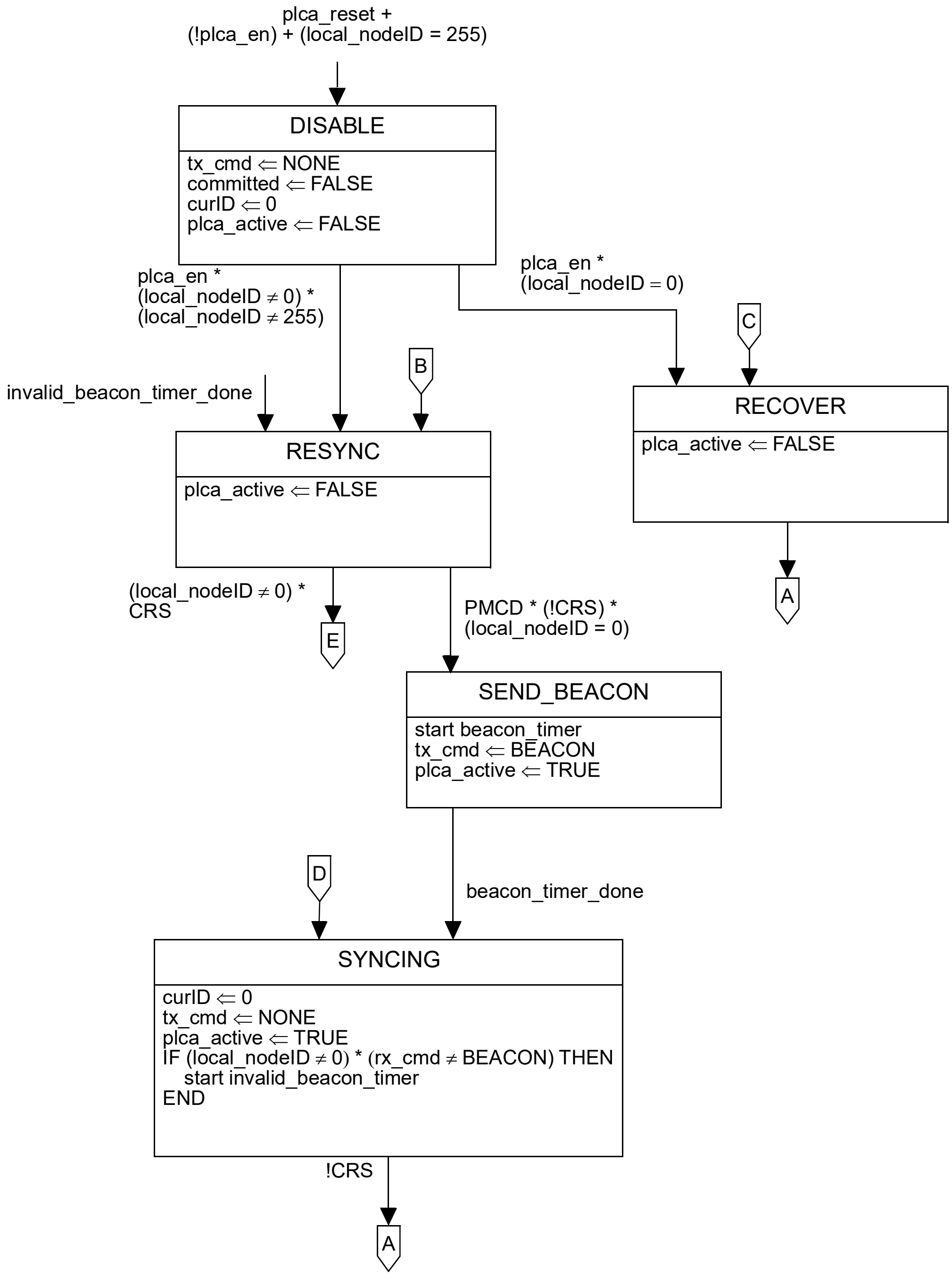


Figure 148–3—PLCA Control state diagram, part a

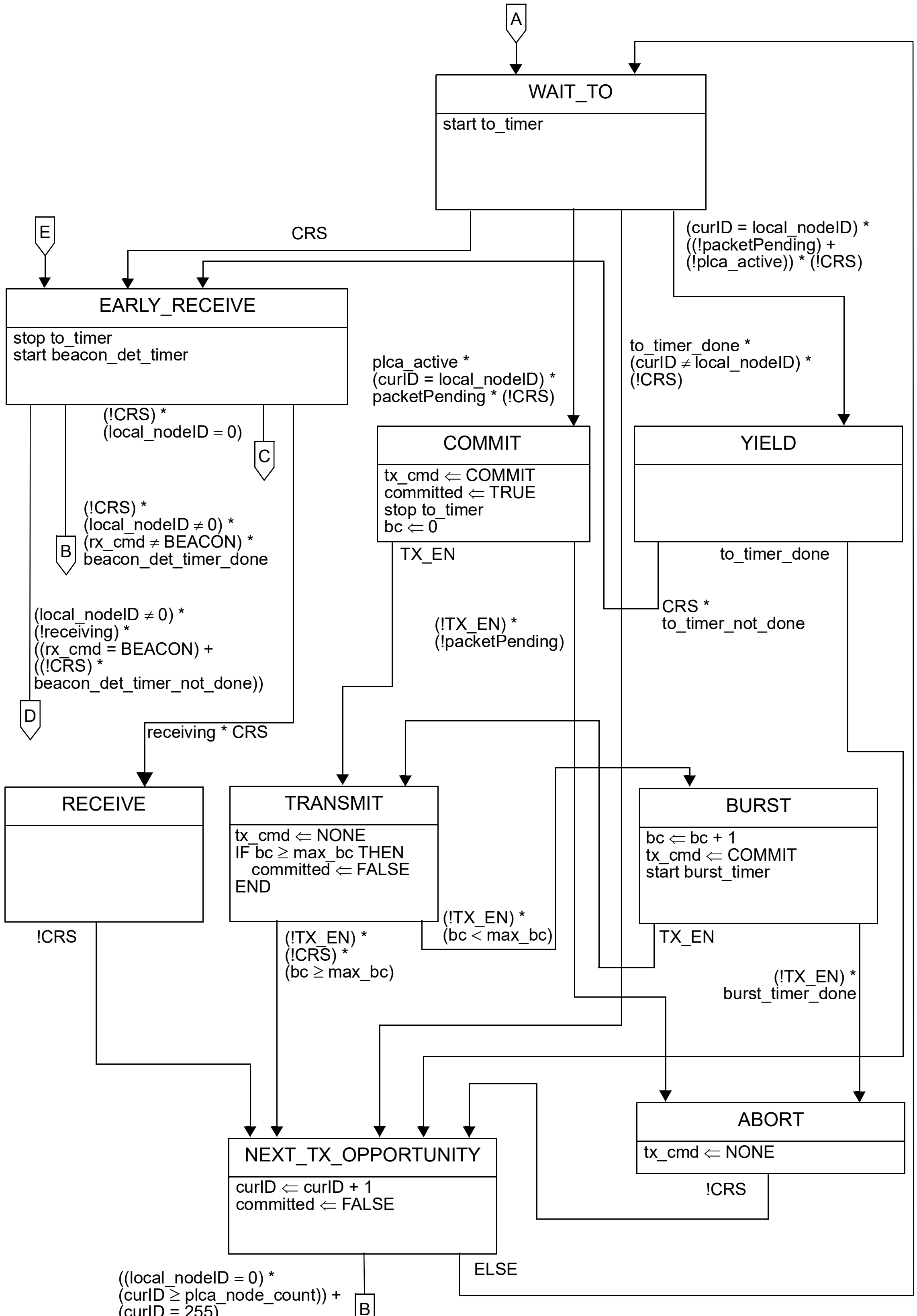


Figure 148–4—PLCA Control state diagram, part b

148.4.5 PLCA Data

148.4.5.1 PLCA Data state diagram

The PLCA Data state diagram is responsible for detecting when the MAC is ready to send a packet and delaying the transmission until a transmit opportunity is detected.

The PLCA Data function shall conform to the PLCA Data state diagram in Figure 148–5 and Figure 148–6 and associated state variables, functions, timers, and messages.

When PLCA functions are enabled, the PLCA Data state diagram transitions to the IDLE state and waits for the MAC to start a transmission or the PHY to assert carrier sense. In the former case, the data conveyed by the MAC through the PLS_DATA.request primitive is delayed by switching to HOLD state. In the latter case, CARRIER_ON is signaled through the PLS_CARRIER.indication to have the MAC defer any new transmission, then the RECEIVE state is entered.

The MAC however, might have started a transmission right before a carrier is detected. In this case, the Data state diagram switches to the COLLIDE state asserting SIGNAL_STATUS = SIGNAL_ERROR via PLS_SIGNAL.indication primitive to have the MAC perform a backoff and send the packet again later, without actually forwarding any data for the PHY to transmit on the medium.

During the HOLD state, the PLCA Control state diagram is notified via the packetPending variable that data is available to be transmitted and the beginning of the transmission is held in the variable delay line. At the next transmit opportunity, the PLCA Control state diagram allows transmitting the delayed data by setting the committed variable to TRUE. In such a case, the PLCA Data state diagram switches to TRANSMIT state to actually deliver the data for the PHY to encode and transmit on the medium.

The variable delay line is a small buffer that aligns a transmission with the transmit opportunity.

If plca_txer is asserted during the HOLD state, the PLCA Data state diagram switches to ABORT state to assert packetPending = FALSE and to wait until the MAC stops sending data. The aborted packet will not be transmitted on the medium.

If another node starts a transmission during the HOLD state, the delayed data is dropped and a collision is triggered by switching to COLLIDE state.

During the COLLIDE state, packetPending = FALSE and CARRIER_STATUS = CARRIER_ON are asserted via the PLS_CARRIER.indication primitive. When the MAC has completed sending the jam bits as described in Clause 4, the PLCA Data state diagram waits for the next transmit opportunity by switching to DELAY_PENDING state. The PLCA Data state diagram transitions to the PENDING state after waiting for the pending_timer. The pending_timer is used to prevent committing to a transmit opportunity before transmit data is available. This prevents conveying unwanted long COMMIT requests to the PHY.

During the PENDING state, the PLCA Data state diagram asserts packetPending = TRUE and keeps CARRIER_STATUS = CARRIER_ON via the PLS_CARRIER.indication primitive to prevent the MAC from making new transmit attempts until the PLCA Control state diagram signals that a new transmit opportunity is available. At that point, CARRIER_STATUS is set to CARRIER_OFF to have the MAC resend data after waiting one IPG period as described in Clause 4.

148.4.5.2 Variables

a
: Current delay counter.

b
: Flush counter.

CARRIER_STATUS
: See 148.4.2.3.2.

COL
: The MII signal COL specified in 22.2.2.12.

committed
: See 148.4.4.2.

CRS
: The MII signal CRS (see 22.2.2.11).

packetPending
: See 148.4.4.2.

plca_en
: See 148.4.4.2.

plca_reset
: See 148.4.4.2.

plca_status
: See 148.4.6.2.

plca_txd<3:0>
: A four-bit data value conveying a nibble of data to transmit from four successive PLS_-DATA.request(OUTPUT_UNIT) primitives where OUTPUT_UNIT has a value of ONE or ZERO. See 148.4.2.1.2. The addition of a subscript 'n-a', i.e., $plca\_txd_{n-a}$ indicates the plca_txd conveyed ‘a’ mii_clock_timer expirations before the most recent one.

plca_txen
: See 148.4.2.1.2.

plca_txer
: The conditions for generating plca_txer are the same as defined in 22.2.1.6 and 22.2.2.5 for the TX_ER MII signal.
Values: TRUE or FALSE

receiving
: See 148.4.4.2.

rx_cmd
: See 148.4.4.2.

SIGNAL_STATUS
: See 148.4.2.4.2

tx_cmd
: See 148.4.4.2.

tx_cmd_sync
: The value of the tx_cmd variable sampled on the rising edge of the MII TX_CLK.
Values: see tx_cmd in 148.4.4.2

TXD
: The MII signals TXD<3:0> specified in 22.2.2.4.

TX_EN
: The MII signal TX_EN specified in 22.2.2.3.

TX_ER
: The MII signal TX_ER specified in 22.2.2.5.

148.4.5.3 Functions

ENCODE_TXER
: This function takes as its argument the tx_cmd_sync variable defined in 148.4.5.2.
It returns TRUE if tx_cmd_sync is BEACON or COMMIT. Otherwise, it returns the value of the plca_txer variable, defined in 148.4.5.2.

ENCODE_TXD
: This function takes as its argument the tx_cmd_sync variable defined in 148.4.5.2.
If tx_cmd_sync is BEACON, the return value is the TXD encoding defined in Table 22–1 for the BEACON request.
If tx_cmd_sync is COMMIT, the return value is the TXD encoding defined in Table 22–1 for the COMMIT request.
Otherwise, the return value is 0000.

148.4.5.4 Timers

commit_timer
: Defines the maximum time the PLCA Data state machine is allowed to stay in WAIT_MAC state.
Duration: 288 bit times.
Tolerance: ± ½ bit time.

mii_clock_timer
: A continuous free-running timer that shall expire synchronously with the rising edge of the MII TX_CLK.
Restart time: Immediately after expiration; restarting the timer resets the condition mii_clock_timer_done.
Duration: see 22.2.2.1.

pending_timer
: Defines the time the PLCA Data state diagram waits in the DELAY_PENDING state before switching to PENDING state.
Duration: 512 bit times.
Tolerance: ± ½ bit time.

148.4.5.5 Abbreviations

MCD Alias for mii_clock_timer_done

148.4.5.6 Constants

delay_line_length
: This constant is implementation dependent and specifies the maximum number of nibbles that the PLCA RS variable delay line can hold.
Value: up to 99

148.4.5.7 State diagram

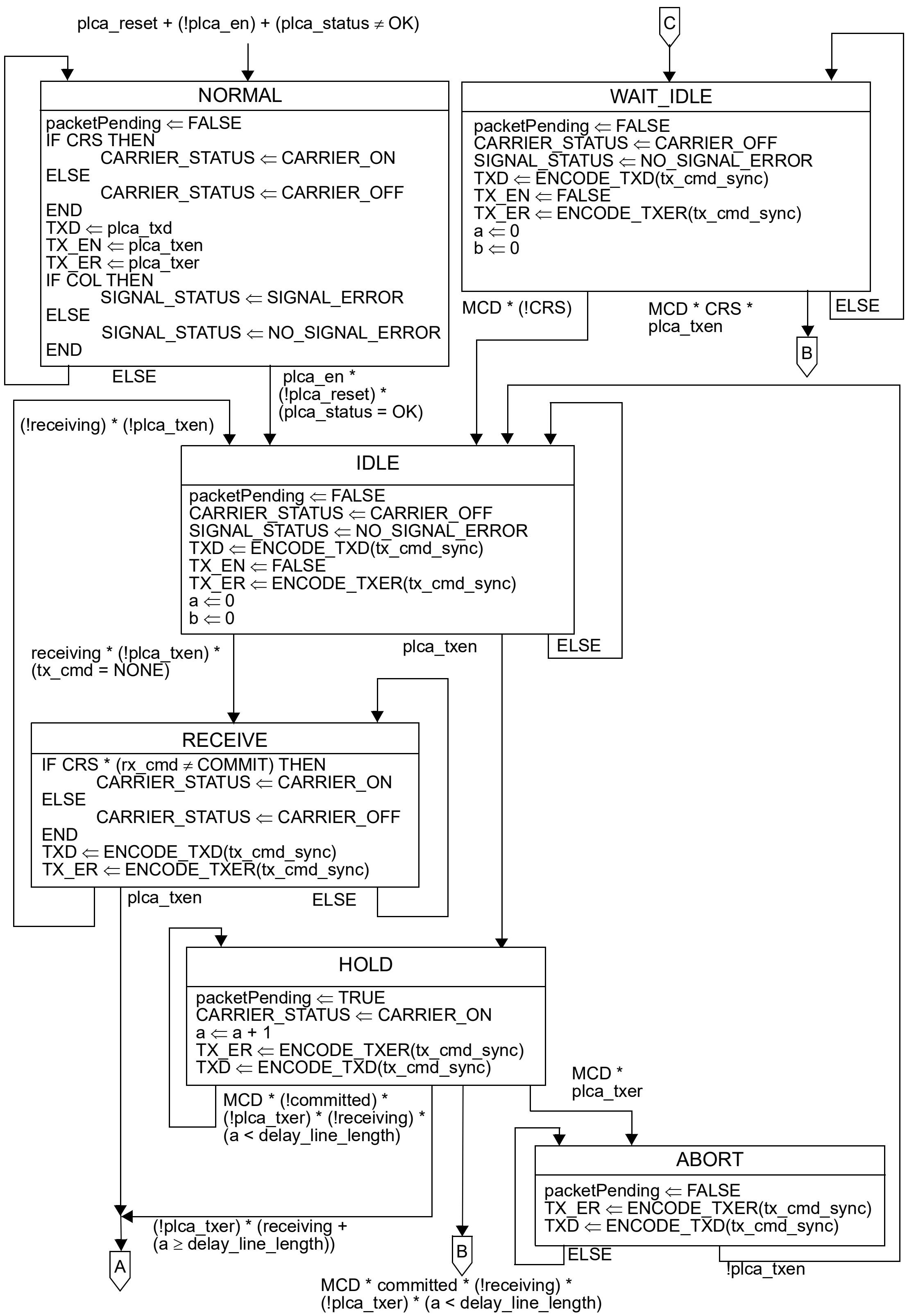


Figure 148–5—PLCA Data state diagram, part a

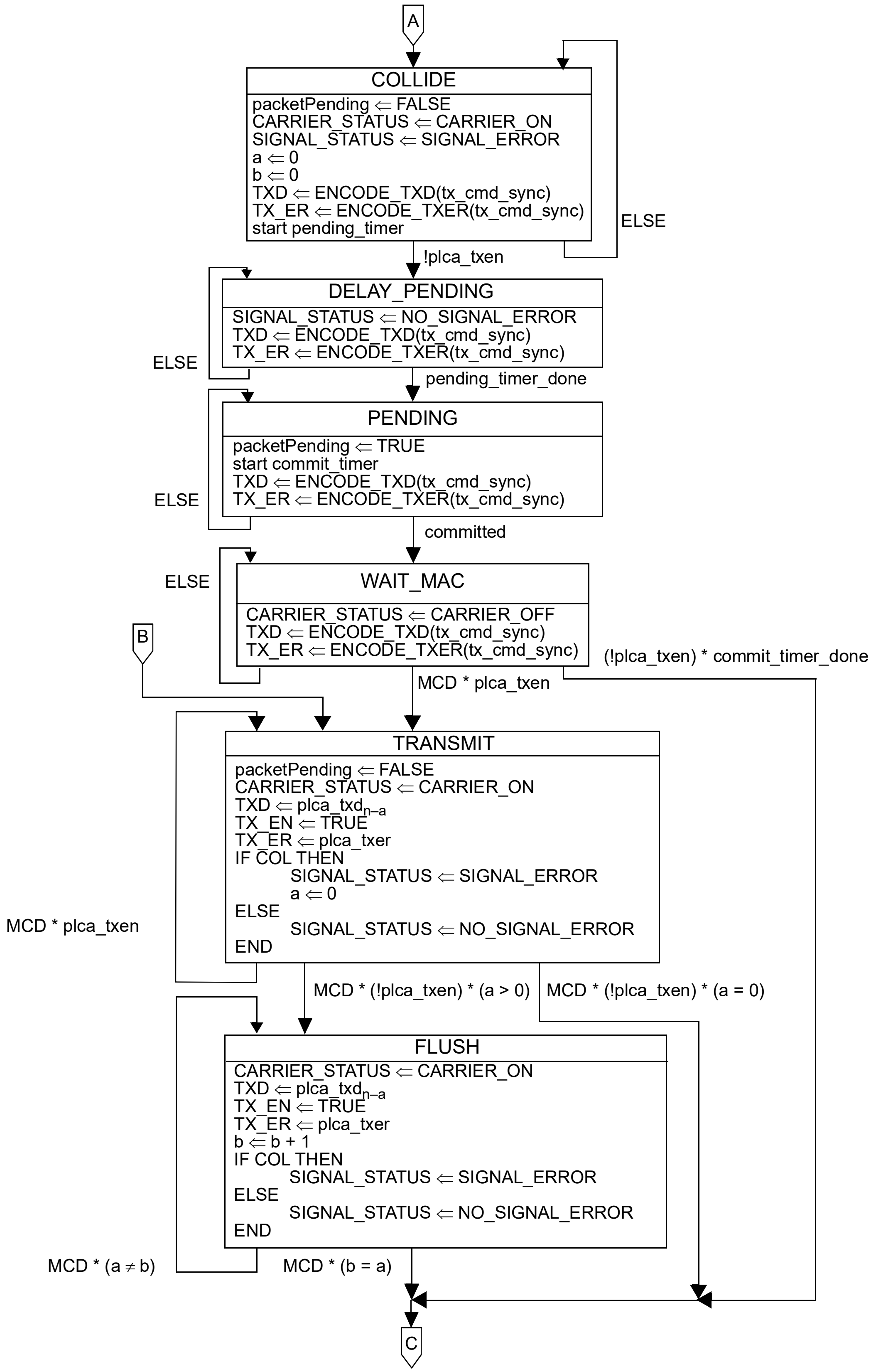


Figure 148–6—PLCA Data state diagram, part b

148.4.6 PLCA Status

148.4.6.1 PLCA Status state diagram

The PLCA Status state diagram is responsible for reporting whether nodes are actively sending/receiving the BEACON. The PLCA Status function shall conform to the PLCA Status state diagram in Figure 148–7 and associated state variables, functions, timers, and messages.

Upon reset or when PLCA is disabled, the PLCA Status function enters the INACTIVE state and reports plca_status as FAIL. As soon as the PLCA Control function enters the SYNCING state (i.e., receiving or transmitting the BEACON), the plca_active variable is set to TRUE and PLCA Status switches to the ACTIVE state, reporting plca_status as OK.

From the ACTIVE state, whenever plca_active is set to FALSE by the PLCA Control function, the PLCA Status function enters the HYSTERESIS state, still reporting plca_status as OK and arming plca_status_timer.

If plca_active is reset to TRUE, then PLCA Status reverts to the ACTIVE state, effectively filtering the momentarily inactive state. Instead, if plca_status_timer expires while plca_active is still FALSE, the PLCA Status function reverts to the INACTIVE state, reporting plca_status as FAIL.

148.4.6.2 PLCA Status variables

plca_status
: If plca_status is OK, BEACONs are being received or transmitted, and the PLCA Control state diagram is in normal operation. If plca_status is FAIL, the PLCA Control state diagram has been in the DISABLE, RESYNC, or RECOVER state for greater than the duration of the plca_status timer. This signal maps to aPLCAStatus attribute as specified in 30.16.1.1.2.
Values: OK or FAIL

plca_active
: See 148.4.4.2.

plca_en
: See 148.4.4.2.

plca_reset
: See 148.4.4.2.

148.4.6.3 Functions

No functions are defined for PLCA Status state diagram.

148.4.6.4 Timers

plca_status_timer
: Represents the time plca_status is maintained in OK state when plca_active is FALSE while in the HYSTERESIS state.
Duration: the duration of this timer is 130 090 bit times, which is 2 × (max to_timer × max plca_node_count + beacon_timer).
Tolerance: timer may expire up to 10 000 BT (nominally 1 ms at 10 Mb/s) greater than the specified duration

148.4.6.5 State diagram

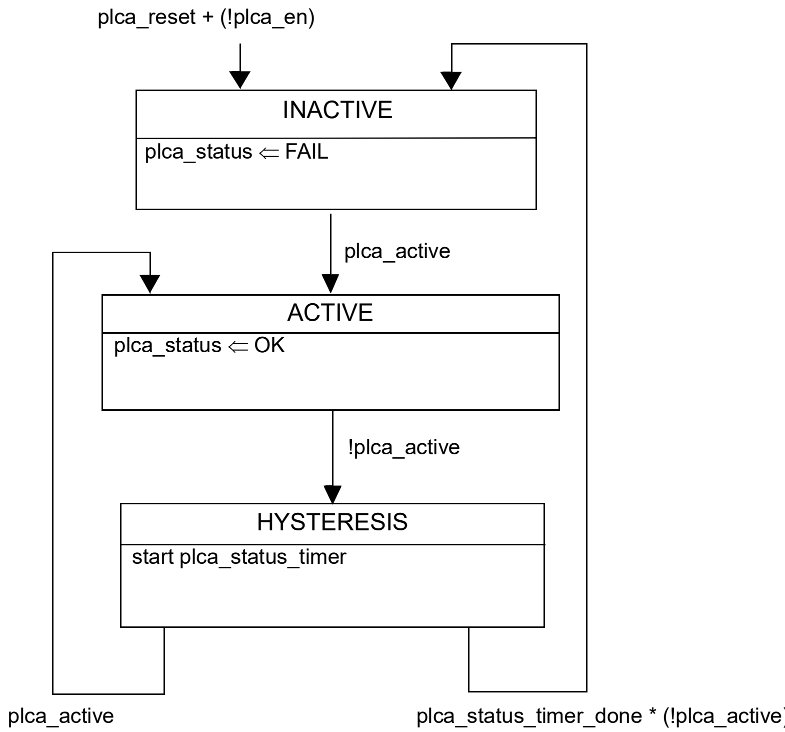


Figure 148–7—PLCA Status state diagram

148.5 Protocol implementation conformance statement (PICS) proforma for Clause 148, PLCA Reconciliation Sublayer (RS)[1]

148.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 148, PLCA Reconciliation Sublayer (RS), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

148.5.2 Identification

148.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

148.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cg-2019, Clause 148, PLCA Reconciliation Sublayer (RS)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cg-2019.)	

Date of Statement	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

148.5.3 PICS proforma tables for PLCA Reconciliation Sublayer (RS)

148.5.3.1 Reconciliation Sublayer

Item	Feature	Subclause	Value/Comment	Status	Support
RS1	PLCA not supported or disabled by management interface	148.4.1	Conform to MII RS definition in Clause 22	M	Yes [ ]

148.5.3.2 Mapping of MII signals to PLS service primitives and PLCA functions

Item	Feature	Subclause	Value/Comment	Status	Support
MAP1	Mapping of PLS_DATA.request when PLCA is disabled	148.4.2.1	Specified in 22.2.1.1	M	Yes [ ]
MAP2	Mapping of PLS_DATA.indication	148.4.2.2	Specified in 22.2.1.2	M	Yes [ ]
MAP3	Mapping of PLS_CARRIER.indication when PLCA is disabled	148.4.2.3	Specified in 22.2.1.3	M	Yes [ ]
MAP4	Mapping of PLS_CARRIER indication when PLCA is enabled	148.4.2.3.1	Maps the primitive PLS_CARRIER.indication to the PLCA Data state diagram	M	Yes [ ]
MAP5	Mapping of PLS_SIGNAL.indication when PLCA is disabled	148.4.2.4	Specified in 22.2.1.4	M	Yes [ ]
MAP6	Mapping of PLS_SIGNAL.indication when PLCA is enabled	148.4.2.4.1	Map the primitive PLS_SIGNAL.indication to the PLCA Data state diagram	M	Yes [ ]
MAP7	Mapping of PLS_DATA_VALID.indicatio n	148.4.2.5	Specified in 22.2.1.7	M	Yes [ ]
MAP8	Generation of TX_ER	148.4.2.6	Specified in 148.4.5.1	M	Yes [ ]
MAP9	Response to RX_ER indication	148.4.2.7	Specified in 22.2.1.5	M	Yes [ ]

148.5.3.3 Specific RS and PHY specification

Item	Feature	Subclause	Value/Comment	Status	Support
PLCA1	RS reaction to BEACON indication reception	148.4.3.2.1	PLCA variable rx_cmd is set to the value BEACON	M	Yes [ ]
PLCA2	RS reaction when BEACON indication ceases	148.4.3.2.1	PLCA variable rx_cmd is reset to NONE unless a COMMIT indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.2	M	Yes [ ]
PLCA3	RS reaction to COMMIT indication reception	148.4.3.2.2	PLCA variable rx_cmd is set to the value COMMIT	M	Yes [ ]
PLCA4	RS reaction when COMMIT indication ceases	148.4.3.2.2	PLCA variable rx_cmd is reset to NONE unless a BEACON indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.1	M	Yes [ ]

148.5.3.4 PLCA Control

Item	Feature	Subclause	Value/Comment	Status	Support
CON1	PLCA Control function	148.4.4.1	Conform to Figure 148–3 and Figure 148–4	M	Yes [ ]

148.5.3.5 PLCA Data

Item	Feature	Subclause	Value/Comment	Status	Support
DAT1	PLCA Data function	148.4.5.1	Conforms to Figure 148–5 and Figure 148–6	M	Yes [ ]

148.5.3.6 PLCA Status

Item	Feature	Subclause	Value/Comment	Status	Support
STS1	PLCA Status function	148.4.6.1	Conforms to Figure 148–7	M	Yes [ ]

Annex A

(informative)

Bibliography

Insert the following references after [B39]:

[B39a] IEC 63171-1 (draft 48B/2783/FDIS, 17 Jan. 2020), Connectors for electrical and electronic equipment—Part 1: Detail specification for 2-way, shielded or unshielded, free and fixed connectors: mechanical mating information, pin assignment and additional requirements for TYPE 1 / Copper LC style.

[B39b] IEC 63171-6:2020, Connectors for electrical and electronic equipment—Part 6: Detail specification for 2-way and 4-way (data/power), shielded, free and fixed connectors for power and data transmission with frequencies up to 600 MHz.

Annex 98B

(normative)

IEEE 802.3 Selector Base Page definition

98B.3 Technology Ability Field bit assignments

Change Table 98B-1 as follows:

Table 98B–1—Technology Ability Field bit assignments

bit	Selector description
A0	100BASE-T1 ability
A1	~~Reserved~~10BASE-T1S full duplex ability
A2	1000BASE-T1 ability
A3 through A8	Reserved
A9	10BASE-T1L capability
A10 through A21	Reserved
A22	10BASE-T1S half duplex capability
A23	10BASE-T1L increased transmit level request
A24	10BASE-T1L increased transmit/receive level ability
A25	10BASE-T1L EEE ability
~~A3 through~~ A26	Reserved

Insert the following new subclause (98B.3.1) after 98B.3:

98B.3.1 10BASE-T1L-specific bit assignments

Configuration of 10BASE-T1L specific bits A23, A24, and A25 are specified in 146.6.

98B.4 Priority Resolution

Change the priority resolution list in 98B.4 as follows:

— 1000BASE-T1
— 100BASE-T1
— 10BASE-T1S full duplex
— 10BASE-T1S half duplex
— 10BASE-T1L

Insert Annex 146A and Annex 146B in alphanumeric order (see earlier in this amendment for the addition of the corresponding clause):

Annex 146A

(informative)

Guidelines for implementation of the 10BASE-T1L PHY in an intrinsically safe application

The principle of intrinsic safety is based on the limitation of voltage, current, power, capacitance, and inductance of electrical circuits. Within hazardous locations, a circuit following the limits of the intrinsic safety standards will not be able to ignite gas or dust atmospheres in case of a short circuit or any other kind of failure.

The additional requirements to achieve equipment protection by intrinsic safety are described by International Standards (e.g., IEC 60079-11). Possible limits of parameters used for intrinsically safe communication circuits can be derived from these standards. The specification of 10BASE-T1L in Clause 146 is intended to be compatible with implementation of such intrinsically safe systems.

In addition, the PHY implementation has a strong impact on intrinsic safety, while using external and discrete components for intrinsic safety related aspects simplifies the certification process. The following implementation choices can simplify the process for certifying 10BASE-T1L PHYs in intrinsically safe systems:

External termination resistors: These can be used to limit the energy and current to or from the intrinsically safe link segment;

Providing separate high impedance receive pins: External resistors for current and energy limitation can also be added to the receive path.

Figure 146A–1 and Figure 146A–2 show, in principle, two possible implementations on how to feed power onto an intrinsically safe link segment. The circuits should be seen only as examples. It is in the responsibility of the hardware designer to fulfill all relevant standards (especially IEC 60079-0 and IEC 60079-11, but also others), when implementing devices for the use within intrinsically safe applications.

NOTE—The version shown in Figure 146A–2 may be easier to implement within a PHY IC as the hybrid within the PHY IC does not need to adapt to different external resistor values.

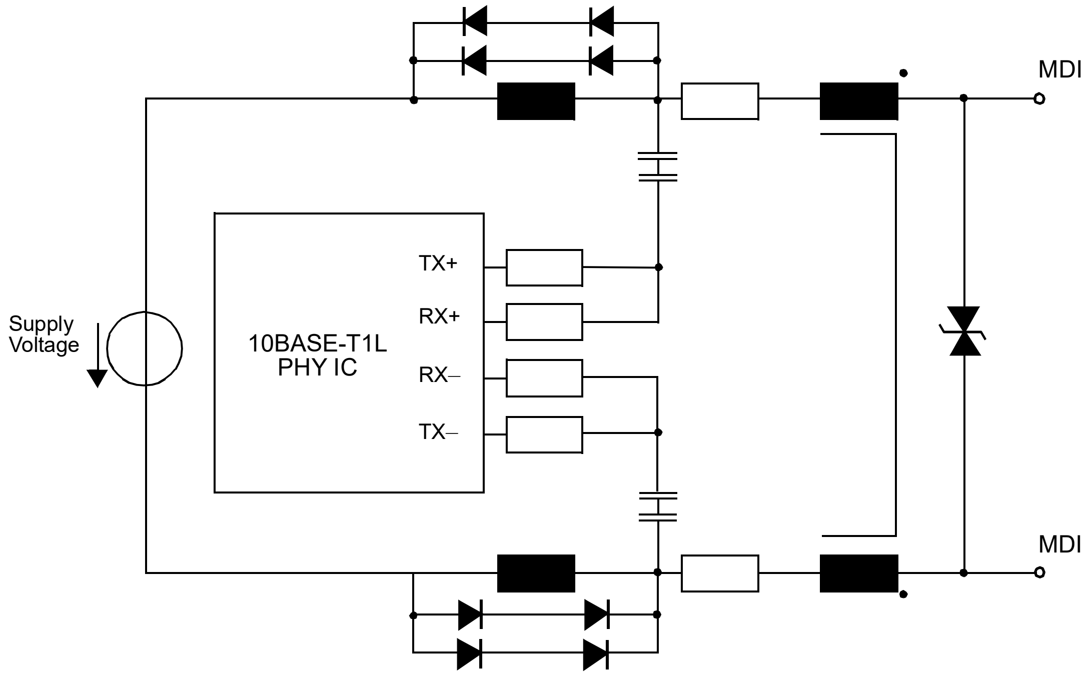


Figure 146A–1—First possible implementation on intrinsically safe power feeding

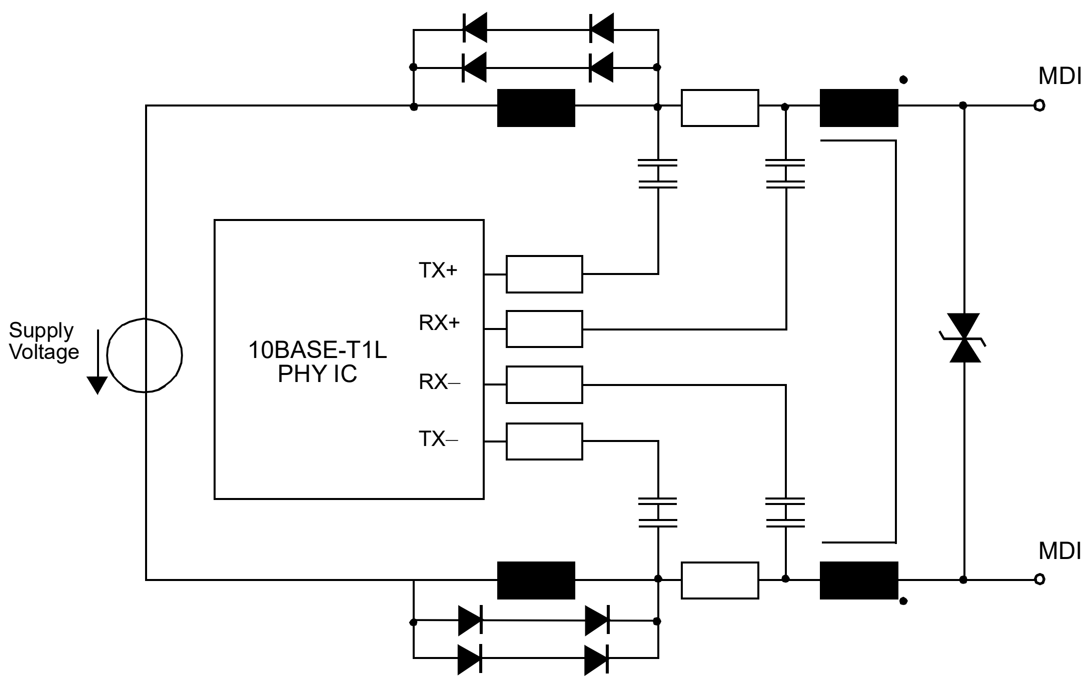


Figure 146A–2—Second possible implementation on intrinsically safe power feeding

Figure 146A–3 shows, in principle, a possible implementation on how to decouple the power from an intrinsically safe link segment. The circuits should be seen only as examples, and values of the components are implementation and application dependent. It is in the responsibility of the hardware designer to fulfill all relevant standards (especially IEC 60079-0 and IEC 60079-11, but also others), when implementing devices for the use within intrinsically safe applications.

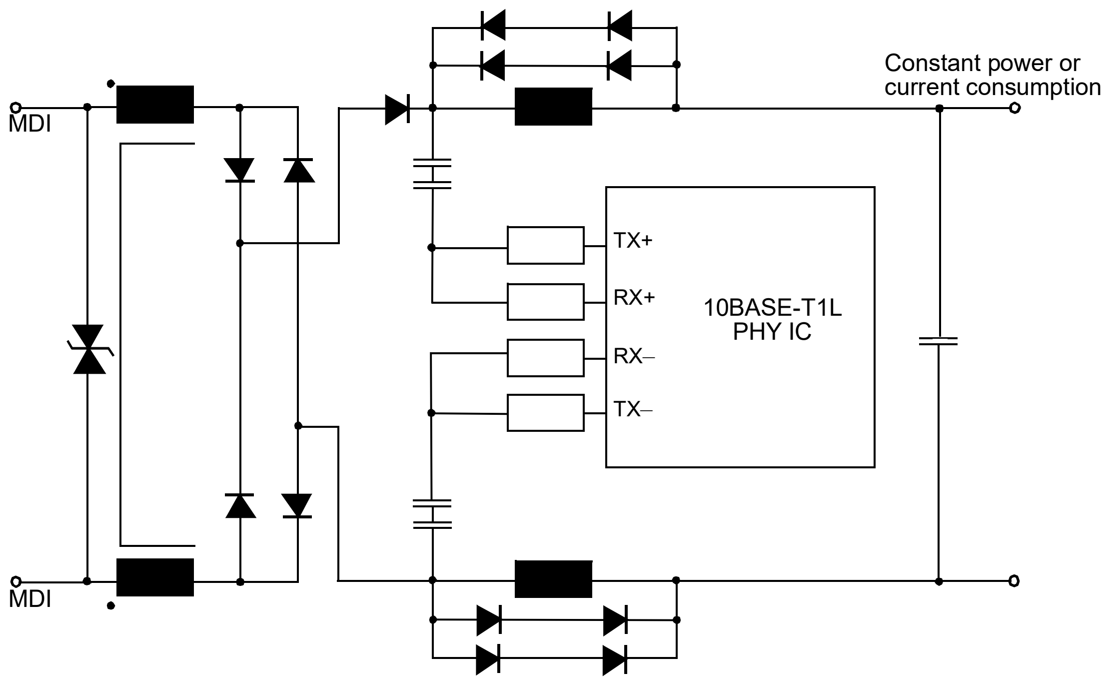


Figure 146A–3—Possible implementation for power decoupling from an intrinsically safe link segment

Annex 146B

(informative)

Optional power distribution

146B.1 Overview

Annex 146B provides information on the optional powering topologies. The class power requirements are specified in Clause 104.

146B.2 Point-to-point powering topologies

The point-to-point powering topology is defined to enable characterization of the direct current resistance (DCR). The point-to-point powering topology is illustrated in Figure 146B–1.

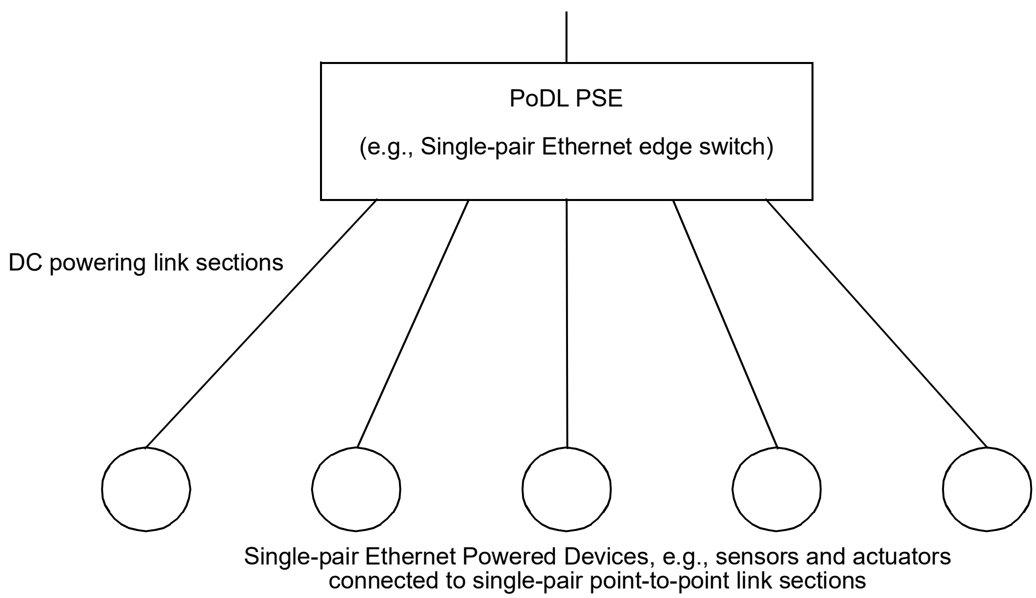


Figure 146B–1—Point-to-point powering topology

The point-to-point link segment DCR characteristics are given in Table 146B–1.

Table 146B–1—Point-to-point link segment DCR characteristics

Conductor diameter mm (AWG)	Resistance per meter (Ω)	Length at IL limit (m)	Conductor resistance at IL limit (Ω)	Loop resistance at IL limit (Ω)	10 connector DCR (Ω)	Link segment resistance at IL limit (Ω)
1.63 (14)	0.0092	1589	14.67	29.33	1	30.33
1.45 (15)	0.0116	1415	16.47	32.94	1	33.94
1.29 (16)	0.0147	1261	18.50	37.00	1	38.00
1.14 (17)	0.0185	1123	20.78	41.55	1	42.55
1.02 (18)	0.0233	1000	23.33	46.66	1	47.66
0.91 (19)	0.0294	891	26.20	52.40	1	53.40
0.81 (20)	0.0371	793	29.42	58.84	1	59.84
0.72 (21)	0.0468	706	33.04	66.07	1	67.07
0.64 (22)	0.0590	629	37.10	74.19	1	75.19
0.57 (23)	0.0744	560	41.66	83.31	1	84.31
0.51 (24)	0.0938	499	46.78	93.55	1	94.55
0.40 (26)	0.1492	395	58.98	117.96	1	118.96

146B.3 Powered trunk cable topologies

The "powered trunk cable" topology is illustrated in Figure 146B–2. The trunk link section provides power to the single pair field switches. The trunk link section can also interconnect field switches. The spur link sections provides power to the PDs. Powering trunk topologies are considered "engineered"; therefore, DCR characteristics for specified lengths are not given.

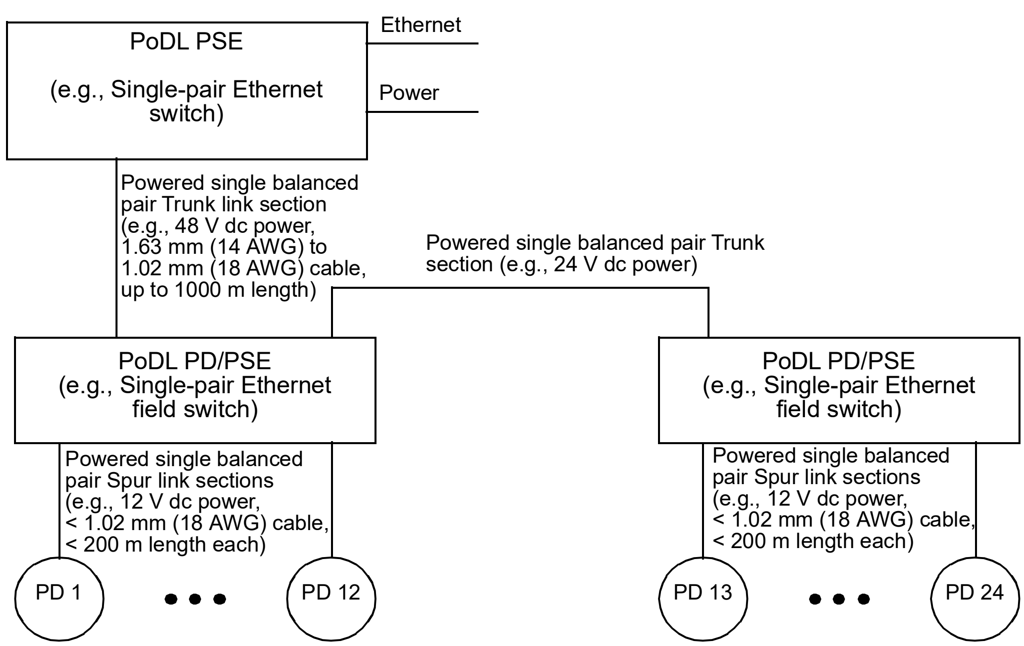


Figure 146B–2—Powered trunk cable topology