ETM37E-06

EPSON
EXCEED YOUR VISION

Application Manual

Real Time Clock Module

RX8010SJ

SEIKO EPSON CORPORATION

ETM37E Revision History

Rev No.	Date	Page	Description
ETM37E-01	14.Jul.2013		Release
ETM37E-02	06.Sep.2013	28	Corrected a setting data of Flow chart Ex2
ETM37E-03	13.Sep.2013	1	Changed a 1. Overview.
		5	Deleted contents of a 8.1 DC characteristics.
		5	Corrected a fCLK to fSCL.
		6	Changed a comment of 8.2.1. AC characteristics.
		7	Deleted a comment of “Target spec”
		7	Deleted a software command of TS sample.
		20,21	Corrected a 13.3. Alarm interrupt Function.
		28	Corrected a setting data of Flow chart Ex2
ETM37E-04	06.Nov.2013	4	Corrected a Item of 7. Frequency Characteristics
		6	Corrected a caution of 8.2.1. AC characteristics(1)
ETM37E-05	13.Dec.2013	12	Changed a 12.2. Register table
		34	Corrected a 13.8.7. The example of the communication wave pattern
ETM37E-06	25.Sep.2014	7,26	Corrected a power-on reset procedure by the software command.

Contents

Low current consumption
SERIAL-INTERFACE REAL TIME CLOCK MODULE

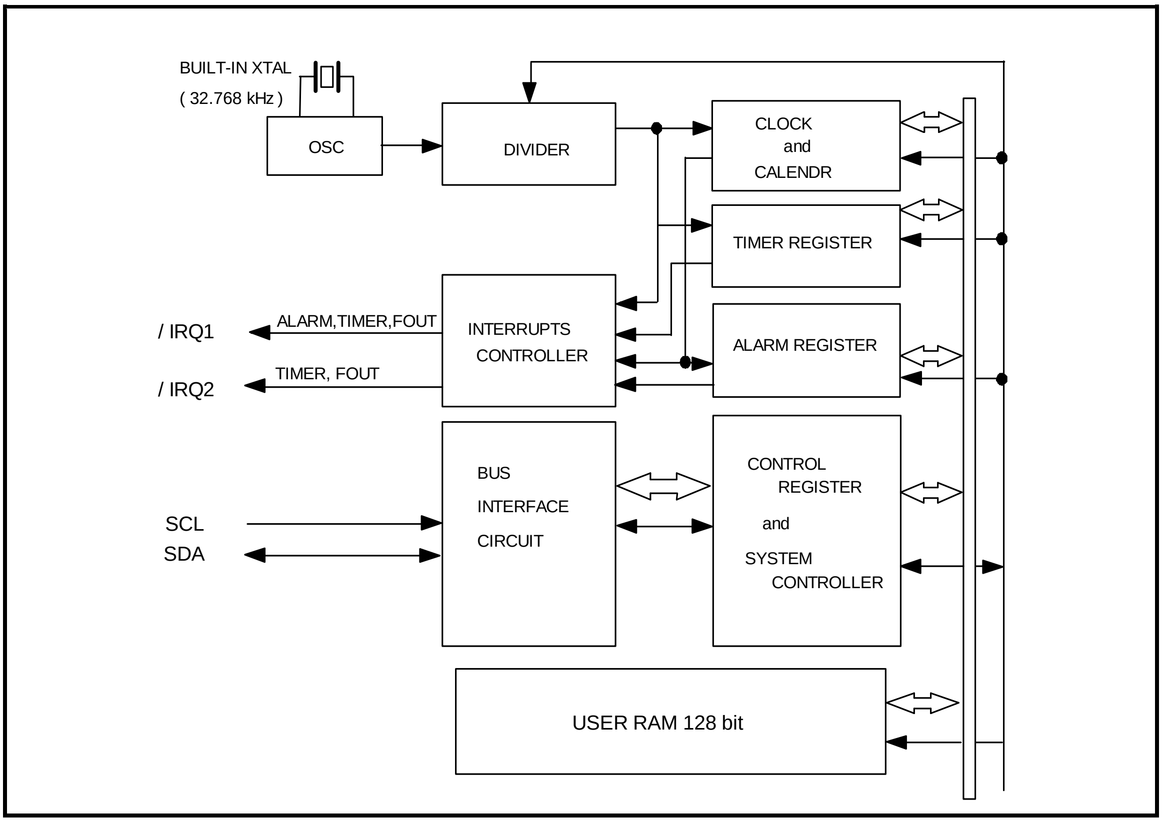
RX8010 SJ

- Built in frequency adjusted 32.768-kHz crystal unit.
- Real-time clock function : Clock/calendar function,Long timer function, alarm interrupt function, etc.
- User RAM : Built in 128 bit RAM
- Frequency output function : 32.768 kHz, 1024 Hz, 1Hz
- Interface type : I^2C-Bus
- Interface voltage range : 1.6 V ~ 5.5 V
- Timekeeper voltage range : 1.1 V ~ 5.5 V
- Backup current consumption : 160 nA $_{Typ}$ / 3 V

1. Overview

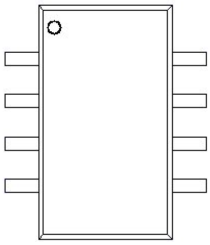
This is a real-time clock module of the serial interface system that incorporates a 32.768 kHz crystal oscillator.
The real-time clock function incorporates not only a calendar and clock counter for the year, month, day, day of the week, hour, minute, and second, but also a time alarm, interval timer, and time update interruption, among other features.
All of these many functions are implemented in a thin, compact SOP package, which makes it suitable for various kinds of small electronic devices.

2. Block Diagram



3. Terminal description

3.1. Terminal connections



SOP – 8pin

3.2. Pin Functions

Signal name	I/O	Function
SCL	Input	This is a shift clock input pin for serial data transmission.
SDA	Input/Output	This is the data input/output pin for serial data transfer.
/ IRQ1	Output	This pin outputs interrupt signals ("L" level) for alarm, timer, time update, and FOUT. This is an N-ch open-drain output.
/ IRQ2	Output	This pin outputs interrupt signals ("L" level) for timer and FOUT. This is a C-MOS output.
VDD	Supply	This is a power-supply pin.
GND	Supply	This pin is connected to a ground.

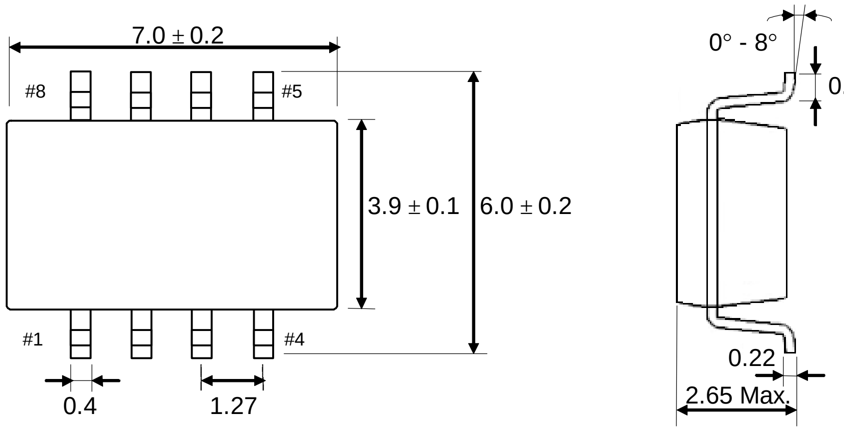
Note: Input pins are able to input up to 5.5V regardless of VDD applied voltage.
Note: Open drain pins are able to Pull-up to 5.5V regardless of VDD applied voltage.
Note: Connect a bypass capacitor rated at least 0.1µF between power supply pins and GND pin.

4. External Dimensions

4.1. External Dimensions

RX8010SJ (SOP – 8 pin)

- External dimensions



Unit : mm

5. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	VDD	Between VDD and GND	–0.3 ~ +6.5	V
Input voltage	VIN	SCL,SDA	–0.3 ~ +6.5	V
Output voltage 1	VOUT1	/IRQ2	–0.3 ~ VDD+0.3	V
Output voltage 2	VOUT2	SDA, /IRQ1	–0.3 ~ +6.5	V
Storage temperature	TSTG	When stored separately, without packaging	–55 to +125	°C

6. Recommended Operating

*Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	VACC	-	1.6	3.0	5.5	V
Clock supply voltage	VCLK	-	1.1	3.0	5.5	V
Low voltage detection	VLOW	-			1.10	V
Applied voltage when OFF	VPUP	SDA, /IRQ1pin			5.5	V
Operating temperature	TOPR	No condensation	–40	+25	+85	°C

*Minimum value of Clock supply voltage VCLK is the timekeeping continuation lower limit value that initialized RX8010 in operating supply voltage VACC.

7. Frequency Characteristics

*Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output frequency	fo			32.768 (Typ.)		kHz
Frequency stability	Δ f / f	Ta = +25 °C VDD = 3.0 V		5 ± 23 (*1)		$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta = +25 °C VDD = 1.2 V ~ 5.5 V	–2		+2	$\times 10^{-6}$ / V
Frequency/temperature characteristics	Top	Ta = –20 °C ~ +70 °C VDD = 3.0 V ; +25 °C reference	–120		+10	$\times 10^{-6}$
Oscillation start time	tSTA	Ta = ±0 °C ~ +50 °C VDD = 1.6 V ~ 5.5 V			1.0	s
		Ta = –40 °C ~ +85 °C VDD = 1.6 V ~ 5.5 V			3.0	s
Aging	fa	Ta = +25 °C , VDD = 3.0 V ; first year	–5		+5	$\times 10^{-6}$ / year

*1) The monthly error is equal to one minute. (excluding offset)

8. Electrical Characteristics

8.1. DC characteristics

*Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

8.1.1. DC characteristics (1)

*Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V ~ 5.5 V , Ta = –40°C ~ +85°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	Input pins are "L" f_{SCL} = 0 Hz, /IRQ1,2 = OFF TSEL2="1"	V_{DD} = 5 V			350	nA
Current consumption (2)	I_{DD2}		V_{DD} = 3 V		160	320	nA
Current consumption (3)	I_{DD3}	f_{SCL} = 0 Hz, /IRQ2 = OFF, /IRQ1 : 32.768 kHz ON	V_{DD} = 5 V		0.60	1.10	µA
Current consumption (4)	I_{DD4}		V_{DD} = 3 V		0.52	0.90	
Current consumption (5)	I_{DD5}	f_{SCL} = 0 Hz, /IRQ1 = OFF, /IRQ2 : 1024 Hz ON , C_L = 15 pF	V_{DD} = 5 V		0.45	1.10	µA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V		0.40	0.90	
High-level input voltage	V_{IH}	SCL,SDA pin		0.8 × V_{DD}		5.5	V
Low-level input voltage	V_{IL}	SCL, SDA pin		GND – 0.3		0.2 × V_{DD}	V
High-level output voltage	V_{OH1}	/IRQ2 pin	V_{DD}=5 V, I_{OH}=–1 mA	4.5		5.0	V
	V_{OH2}		V_{DD} =3 V, I_{OH}=–0.5 mA	2.7		3.0	
Low-level output voltage	V_{OL1}	/IRQ2 pin	V_{DD} =5 V, I_{OL}=1 mA	GND		GND +0.5	V
	V_{OL2}		V_{DD} =3 V, I_{OL}=0.5 mA	GND		GND +0.3	
	V_{OL4}	/IRQ1 pin	V_{DD} =5 V, I_{OL}=1 mA	GND		GND +0.25	V
	V_{OL5}		V_{DD} =3 V, I_{OL}=1 mA	GND		GND +0.4	
Input leakage current	I_{LK}	Input pin, V_{IN} = V_{DD} or GND		–0.1		0.1	µA
Onput leakage current	I_{OZ}	Input pin, V_{OUT} = V_{DD} or GND		–0.1		0.1	µA

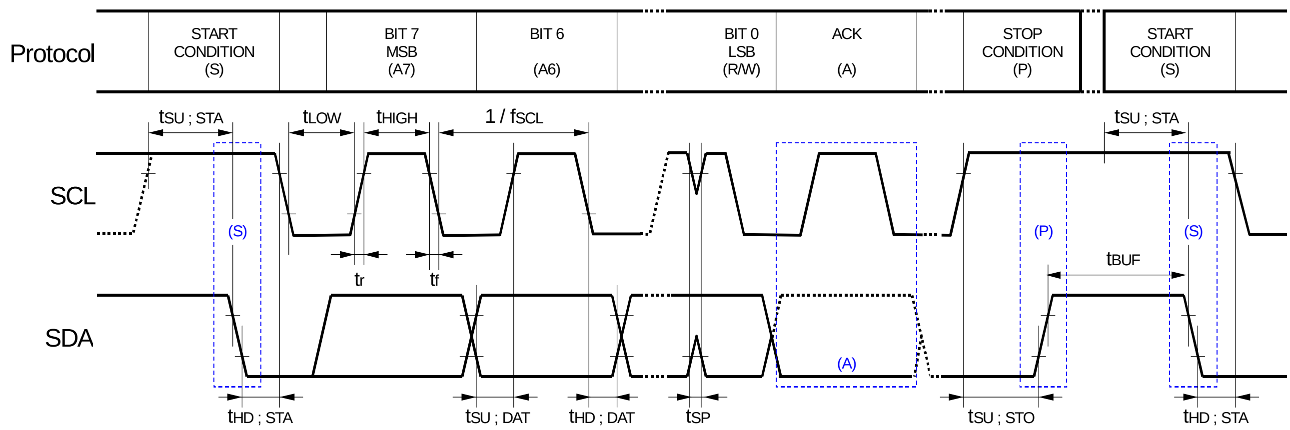
8.2. AC characteristics

8.2.1. AC characteristics(1)

*Unless otherwise specified, GND = 0 V , V_{DD}= 1.6 V ~ 5.5 V , Ta = –40°C ~ +85°C

Item	Symbol	Standard-Mode (f_{SCL}=100kHz)		Fast-Mode (f_{SCL}=400kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Start condition setup time	$t_{SU;STA}$	4.7		0.6		µs
Start condition hold time	$t_{HD;STA}$	4.0		0.6		µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Data hold time	$t_{HD;DAT}$	0		0		ns
Stop condition setup time	$t_{SU;STO}$	4.0		0.6		µs
Bus idle time between start condition and stop condition	t_{BUF}	4.7		1.3		µs
Time when SCL = "L"	t_{LOW}	4.7		1.3		µs
Time when SCL = "H"	t_{HIGH}	4.0		0.6		µs
Rise time for SCL and SDA	t_r		1.0		0.3	µs
Fall time for SCL and SDA	t_f		0.3		0.3	µs
Allowable spike time on bus	t_{SP}		50		50	ns

- Timing chart



Caution: When communication of I^2C-bus is started, consumption electric currents increase.
When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.95 seconds.
If such communication requires 0.95 seconds or longer, the I^2C bus interface is reset by the internal bus timeout function.

8.2.2. AC characteristics (2)

*Unless otherwise specified, GND = 0 V , V_{DD}= 1.6 V ~ 5.5 V , Ta = –40°C ~ +85°C

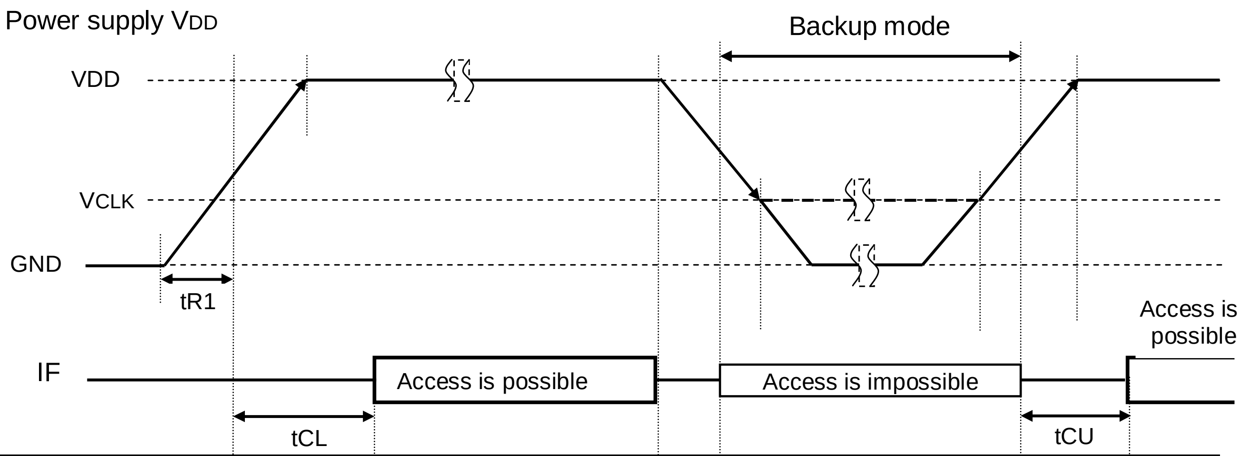
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FOUT symmetry (/IRQ2)	SYM	50% V_{DD} Level	40	50	60	%

9. Matters that demand special attention on use

9.1. Instructions in the power on

9.1.1. Characteristic for the fluctuation of the power supply

∗tR1 is restrictions to validate power-on reset. When cannot keep this standard, power-on reset does not work normally. It is necessary to initial setting by the software command.
Repeated ON/OFF of the power supply in short term, the power-on reset becomes unstable.
After power-OFF, keep a state of VDD=GND more than 60 seconds to validate power-on reset.
When it is impossible, please perform initial setting by the software command.



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	tR1	GND – VDD	1	-	100	µs / V
access wait time (Initial power on)	tCL	-	40	-	-	ms
access wait time (Normal power on)	tCU	-	40	-	-	ms

A power-on reset procedure by the software command

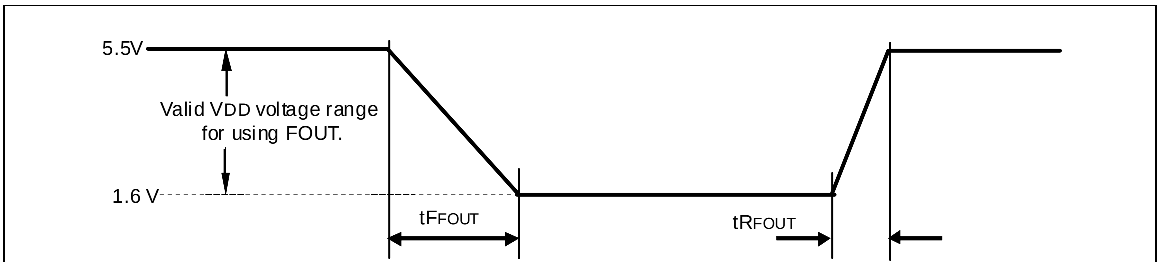
1) Power- on
2) Wait: At least 40ms.
3) Dummy read. ∗1
4) Check VLF bit = "1"
5) Write 00[h] Address:Reg-1F[h]
6) Write 80[h] Address:Reg-1F[h]
7) Write D3[h] Address:Reg-60[h]
8) Write 03[h] Address:Reg-66[h]
9) Write 02[h] Address:Reg-6B[h]
10) Write 01[h] Address:Reg-6B[h]
11) Wait: At least 2ms *2
END

∗1 Dummy read
The location of the address is arbitrary.
Do not check ACK/NACK from RX8010.

∗2 Wait: At least 2ms
This wait time is necessary before transmitting the command for clearing VLF bit after software command transmission.

A disappearance of the FOUT output when the voltage sharply went up and down.

For example, VDD voltage of the RX8010 is come and go between Main power and backup battery.
The clock output from output pins disappears then during several milli-seconds when a sharp voltage change happens.
Please check that there is not a problem by this characteristic on your system.
An reference example of a power up and down timing without affect to FOUT.



tFFOUT Please make speed to descend of a power supply voltage loose than 4 ms/V.
tRFOUT Please make speed to rise of a power supply voltage loose than 4 ms/V.

供电电压不可以快速变化

9.2. Restrictions on Access Operations during Power-on Initialization and Recovery from Backup

- RTC-register operations are linked to the internal quartz oscillator's clock signal, so normal operation is not possible if there is no internal oscillation (= oscillation is stopped).

  Therefore, we recommend that the initial setting to be set during power-on initialization or backup and restore operations (i.e., when the power supply voltage is recovered after oscillation has stopped due to a voltage drop, etc.) should be "first start internal oscillation, then wait for the oscillation stabilization time (see tSTA standard) to elapse".

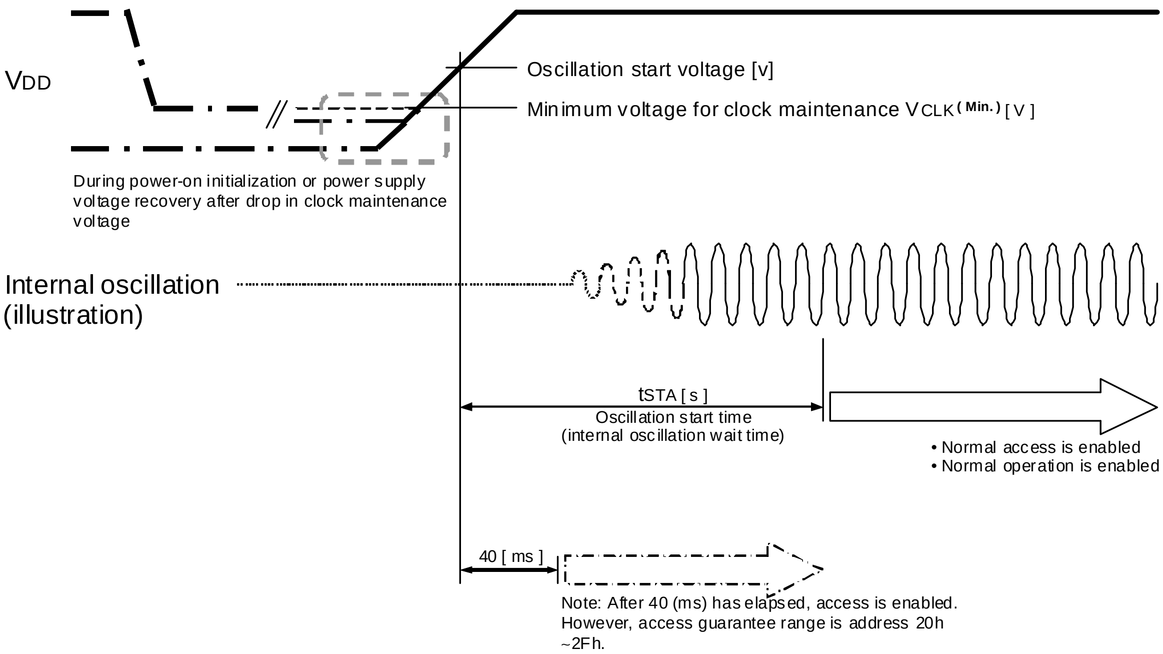
- Note the following caution points concerning access operations during power-on initialization or when restoring the power supply voltage from backup mode (here after referred to as "switching to the operating voltage").

  1) Before switching to the operating voltage, read the VLF-bit (which indicates the RTC error status).

  2) Initialization is required when the value read from the VLF-bit is "VLF = 1 (error status)".
  Before initializing in response to this VLF = "1" result, we recommend first waiting for the internal oscillation stabilization time (see the tSTA standard) to elapse.

Initialization is required when the status after reading a VLF-bit value of "1" is either of the following. (Status 1) During power-on initialization (Status 2) When the clock setting is invalid, such as due to a voltage drop during backup

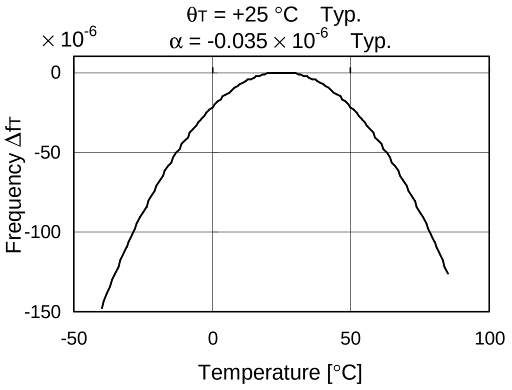
∗ Access timing during power-on initialization and when recovering the power supply voltage after a drop in the voltage used to maintain the clock



10. Reference information

10.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

   $\Delta f_T = \alpha\ (\theta_T - \theta_X)^2$

   - Δf_T : Frequency deviation in any temperature
   - α [1 / °C^2] : Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6}$ / °C^2
   - θ_T [°C] : Ultimate temperature ($+25 \pm 5$ °C)
   - θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

   $\Delta f/f = \Delta f/fo + \Delta f_T + \Delta fv$

   - $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
   - $\Delta f/fo$: Frequency precision
   - Δf_T : Frequency deviation in any temperature.
   - Δfv : Frequency deviation in any voltage.

3. How to find the date difference

   Date Difference = $\Delta f/f \times 86400$(Sec)

   ∗ For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins. Also, avoid placing any device that generates high level of electronic noise near this module.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VIO or GND.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.
* See Fig. 1 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

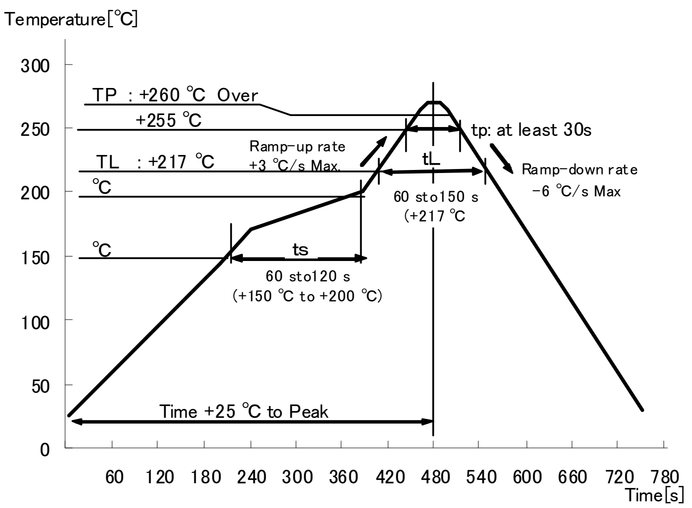
(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Reference profile for our evaluation of Soldering heat resistance.



12. Overview of Functions and Description of Registers

Note:

The initialization of the register is necessary about the unused function and Reserved bit

12.1. Overview of Functions

1) Clock functions

This function is used to set and read out month, day, hour, date, minute, second, and year (last two digits) data. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.
At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.

2) Fixed-cycle Timer Interrupt function

The fixed-cycle timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 µs and 65535 hours.
When an interrupt event is generated, the /IRQ2 pin goes to low level ("L") and "1" is set to the TF bit to report that an event has occurred.

周期定时中断

3) Long-Timer function

It is able to use fixed cycle timer interrupt function as Long-Timer that deals with for approx. 15 years.

4) Alarm interrupt function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ1 pin goes to low level to indicate that an event has occurred.

告警中断

5) Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock. When an interrupt event is generated, the /IRQ1 pin goes to low level ("L") and "1" is set to the UF bit to report that an event has occurred.

6) Frequency stop detection function (VLF-bit)

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop.

7) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the /IRQ1, /IRQ2 pin.

8) User RAM

RAM register is read/write accessible for any data.

12.2. Register table

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	○	40	20	10	8	4	2	1
11	MIN	○	40	20	10	8	4	2	1
12	HOUR	○	○	20	10	8	4	2	1
13	WEEK	○	6	5	4	3	2	1	0
14	DAY	○	○	20	10	8	4	2	1
15	MONTH	○	○	○	10	8	4	2	1
16	YEAR	80	40	20	10	8	4	2	1
17	Reserved	-	-	-	-	-	-	-	-
	Setting data	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**0**
18	MIN Alarm	AE	40	20	10	8	4	2	1
19	HOUR Alarm	AE	•	20	10	8	4	2	1
1A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1B	Timer Counter 0	128	64	32	16	8	4	2	1
1C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	AF	○	VLF	○
1F	Control Register	***TEST***	STOP	UIE	TIE	AIE	TSTP	-	-
	Setting data	**0**	STOP	UIE	TIE	AIE	TSTP	**0**	**0**

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20 | 2F	RAM	User Register 128 bit (16 word x 8 bit)							

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Reserved	-	-	-	-	-	-	-	-
	Setting data	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
31	Reserved	○	○	○	-	-	-	-	-
	Setting data	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
32	IRQ Control	○	-	-	-	○	TMPIN	FOPIN1	FOPIN0
	Setting data	**0**	**0**	**0**	**0**	**0**	TMPIN	FOPIN1	FOPIN0

Note During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.
When doing this, be careful to avoid setting incorrect data as the date or time, as timed operations cannot be guaranteed if incorrect date or time data has been set.

∗1. During the initial power-on (from 0 V), the power-on reset function sets "1" to the VLF bit.
∗ Since the value of other registers is undefined at this time, be sure to reset all registers before using them.

∗2. The ***TEST***, bit are Epson test bits.
∗ Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing.
∗ The four ***TEST**** bits are undefined when read. Those bits should be masked after being read.

∗3. The ' ○ ' mark indicates a write-prohibited bit, which returns a "0" when read.
∗4. The ' • ' mark indicates a read/write-accessible RAM bit for any data.
∗5. The '-' mark is a Reserved bit. It is necessary to write in ***Setting data*** at the time of initialization.
∗6. User Register is a free register.

12.3. Description of registers

12.3.1. Clock and calender counter (Reg - 10[h] ~ 16[h])

This is counter registers from a second to year.

∗ Please refer to [13.1 Clock calendar explanation] for the details.

12.3.2. RAM registers (Reg - 20[h] ~ 2F[h])

This RAM register is read/write accessible for any data in the range from 00 h to FF h.

12.3.3. Alarm registers (Reg - 18[h] ~ 1A[h])

The alarm interrupt function is used, along with the AE, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.

∗ Please refer to [13.3. Alarm Interrupt Function] for the details.

12.3.4. Timer setting and Timer counter register (Reg - 1B[h] ~ 1C[h])

This register is used to set the default (preset) value for the counter.
To use the fixed-cycle timer interrupt function,TE, TF, TIE, TSEL2,TSEL1, TSEL0,TMPIN bits are set and used. When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

∗ Please refer to [13.2. Fixed-cycle Timer Interrupt Function] for the details.

12.3.5. Function-related register 1 (Reg - 1D[h] ~ 1F[h])

1) FSEL1, FSEL0 bit

A combination of the FSEL1 and FSEL0 bits is used to select the frequency to be output.
The choice is possible by a combination of FSEL-bits select the frequency of clock output or inhibits the clock output.

∗ Please refer to [13.6. FOUT Function] for the details.

2) USEL , UF, UIE bit

This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.

∗ Please refer to [13.4. Update interrupt function] for the details.

3) TE, TF, TIE, TSEL2, TSEL1, TSEL0, TSTP bit

These bits are used to control operation of the fixed-cycle timer interrupt function.

4) WADA, AF, AIE bit

These bits are used to control operation of the alarm interrupt function.

5) ***TEST*** bit

Those bits are the manufacturer's test bit. Always leave this bit value as "0" except when testing.

6) VLF bit

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop.

∗ Please refer to [13.5. Frequency stop detection function] for the details.

7) STOP bit

This bit is to stop a timekeeping operation. In the case of “STOP bit = 1", working is as follows a function .

∗ 1) All the update of timekeeping and the calendar operation stops.
With it, an update interrupt event does not occur at an alarm interrupt and the time.

∗ 2) The part of the fixed-cycle timer interrupt function stops.
A count stops the source clock setting of the timer in case of "64Hz, 1Hz, 1min, 1h".

∗ 3) Note 3: The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz output is possible.
But 1Hz and 1024Hz output is disabled.

12.3.6. Function-related register 2 (Reg - 30[h] ~ 32[h])

1)FOPIN1,FOPIN0 bit

This bit selects destination (/IRQ1 or /IRQ2) of FOUT.

2)TMPIN bit

This bit selects destination (/IRQ1 or /IRQ2) of fixed-cycle timer function.

12.3.7. Reservedbit

The ' - ' mark has to write in specified fixed value in the case of initialization by all means.
Writing data as follows.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
17	Reserved	-	-	-	-	-	-	-	-
	Setting data	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**0**
1F	Control Register	***TEST***	STOP	UIE	TIE	AIE	TSTP	-	-
	Setting data	**0**	STOP	UIE	TIE	AIE	TSTP	**0**	**0**

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Reserved	-	-	-	-	-	-	-	-
	Setting data	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
31	Reserved	○	○	○	-	-	-	-	-
	Setting data	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
32	IRQ Control	○	-	-	-	○	TMPIN	FOPIN1	FOPIN0
	Setting data	**0**	**0**	**0**	**0**	**0**	TMPIN	FOPIN1	FOPIN0

The ' ○ ' mark indicates a write-prohibited bit, which returns a "0" when read.

13. How to use

13.1. Clock calendar explanation

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end. Therefore it recommends that the access to a clock calendar has continuous access by the auto increment function.

Setting example: Sun, 29-Feb-88 17:39:45 (leap year)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	1	0	0	0	1	0	1
11	MIN	0	0	1	1	1	0	0	1
12	HOUR	0	0	0	1	0	1	1	1
13	WEEK	0	0	0	0	0	0	0	1
14	DAY	0	0	1	0	1	0	0	1
15	MONTH	0	0	0	0	0	0	1	0
16	YEAR	1	0	0	0	1	0	0	0

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

13.1.1. Clock counter

1) [SEC] [MIN] register

These registers are 60-base BCD counters. These registers are incremented at the timing when carry is generated from a lower register. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.

When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512Hz ~ 1 Hz) is cleared to 0.

2) [HOUR] register

This register is a 24-base BCD counter (24 hour format).These registers are incremented at the timing when carry is generated from a lower register.

13.1.2. Week counter

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.

The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.

It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.

The setting example of the week register value.

Day	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Data [h]
Sunday	0	0	0	0	0	0	0	**1**	01 h
Monday	0	0	0	0	0	0	**1**	0	02 h
Tuesday	0	0	0	0	0	**1**	0	0	04 h
Wednesday	0	0	0	0	**1**	0	0	0	08 h
Thursday	0	0	0	**1**	0	0	0	0	10 h
Friday	0	0	**1**	0	0	0	0	0	20 h
Saturday	0	**1**	0	0	0	0	0	0	40 h

∗ Do not set "1" to more than one day at the same time.

13.1.3. Calendar counter

1) [DAY], [MONTH] resister

The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is 12-base BCD counter. when carry is generated from a lower register.

		Jan.	Feb.	Mar	Apr.	May	June	July	Aug.	Sep.	Oct.	Nov.	Dec.
Days	Normal year	31	28	31	30	31	30	31	31	30	31	30	31
	Leap year		29										

2) [YEAR] register

This register is a BCD counter for years 00 to 99.

The leap year is automatically determined, which reflects in the DAY register.

13.2. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt function generates an interrupt event periodically at any fixed cycle set between

244.14 µs and 65535 hours. This function can stop at one time and is available as a accumulative timer.
After the interrupt occurs, the /IRQ status is automatically cleared .

13.2.2. Related registers for function of fixed-cycle timer interrupt function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
1C	Timer Counter 1	**32768**	**16384**	**8192**	**4096**	**2048**	**1024**	**512**	**256**
1D	Extension Register	FSEL1	FSEL0	USEL	**TE**	WADA	**TSEL2**	**TSEL1**	**TSEL0**
1E	Flag Register	○	○	UF	**TF**	AF	○	VLF	○
1F	Control Register	***TEST***	STOP	UIE	**TIE**	AIE	**TSTP**	-	-

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
32	IRQ Control	O	-	-	-	O	**TMPIN**	FOPIN1	FOPIN0

* Before entering operation settings, we recommend first clearing the TE bit to "0" .
* When the fixed-cycle timer function is not being used, the fixed-cycle Timer Counter0,1 register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) Down counter for fixed-cycle timer (Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1 (0001 h) to 65535 (FFFFh) can be set.
Be sure to write "0" to the TE bit before writing the preset value.

* When TE=0, read out data of timer counter is default(Preset) value.
And when TE=1, read out data of timer counter is just counting value.
But, when access to timer counter data, counting value is not held.
Therefore, for example, perform twice read access to obtain right data, and a way to adopt the case that two data accorded is necessary.

2) TSEL2, TSEL1, TESL0 bit

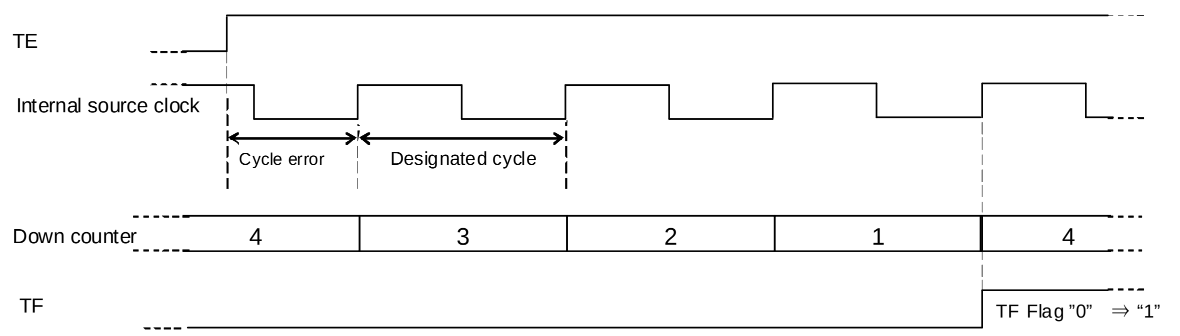
The combination of these three bits is used to set the countdown period (source clock) for this function.

TSEL2 (bit 2)	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN
0	0	0	4096 Hz /Once per 244.14 µs	122 µs
0	0	1	64 Hz /Once per 15.625 ms	7.813 ms
0	1	0	1 Hz /Once per second	7.813 ms
0	1	1	1/60 Hz /Once per minute	7.813 ms
1	0	0	1/3600 Hz /Once per hour	7.813 ms

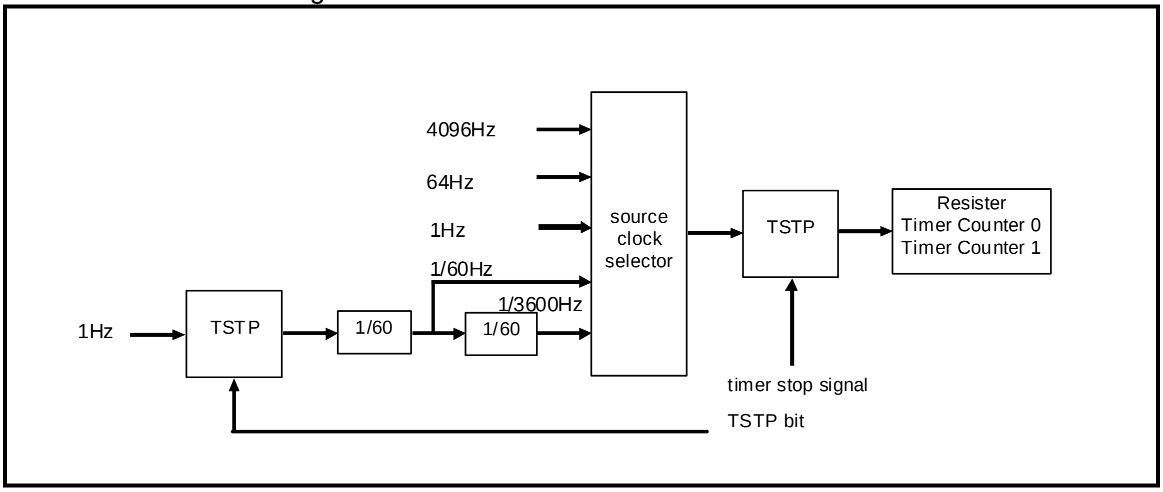
*1) The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

*2) The first countdown shortens than a source clock.
When selected 4,096Hz / 64HZ / 1Hz as a source clock, one period of error occurs at the maximum.
When selected1/60Hz / 1/3600Hz as a source clock, 1Hz of error occurs at the maximum.

The example of the error of the first countdown: A value to preset is 0004h



Inside counter block diagram



＊ Cannot read the count value that is lower than a selected source clock.

3) TE bit (Timer Enable)

When TE bit is "0", the default (preset) can be checked by reading this register.

TE	Data	Description
Write	0	Stops fixed-cycle timer interrupt function. ＊ Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z).
	1	Starts fixed-cycle timer interrupt function. ＊ The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection ＊ Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z).
	1	This bit is invalid after a "1" has been written to it.
Read	0	–
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ1 or /IRQ" pin when a fixed-cycle timer interrupt event has occurred.

TIE	Data	Description
Write	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated. 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-z to low).

7) TSTP bit (Timer Stop)

This bit is used to stop fixed-cycle timer count down.

operation	STOP	TSTP	Description
Write	0	0	Writing a "0" to this bit cancels stop status (restarts timer count down). ∗The reopening value of the countdown is a stopping value
		1	Count stops.
	1	X	The count stops at the time of the setting of 64Hz, 1Hz,1/60Hz,1/3600Hz.

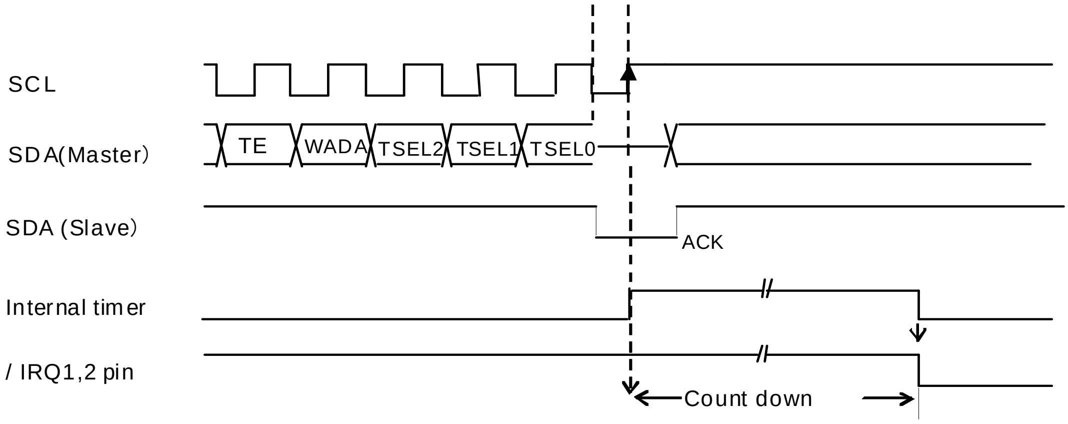
8) TMPIN bit

Select the destination of the timer interrupt output signal.(/IRQ1 or /IRQ2)

TMPIN	Data	Description
Write	0	/IRQ2 pin
	1	/IRQ1 pin

13.2.3. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL (ACK output) signal that occurs when the TE value is changed from "0" to "1".

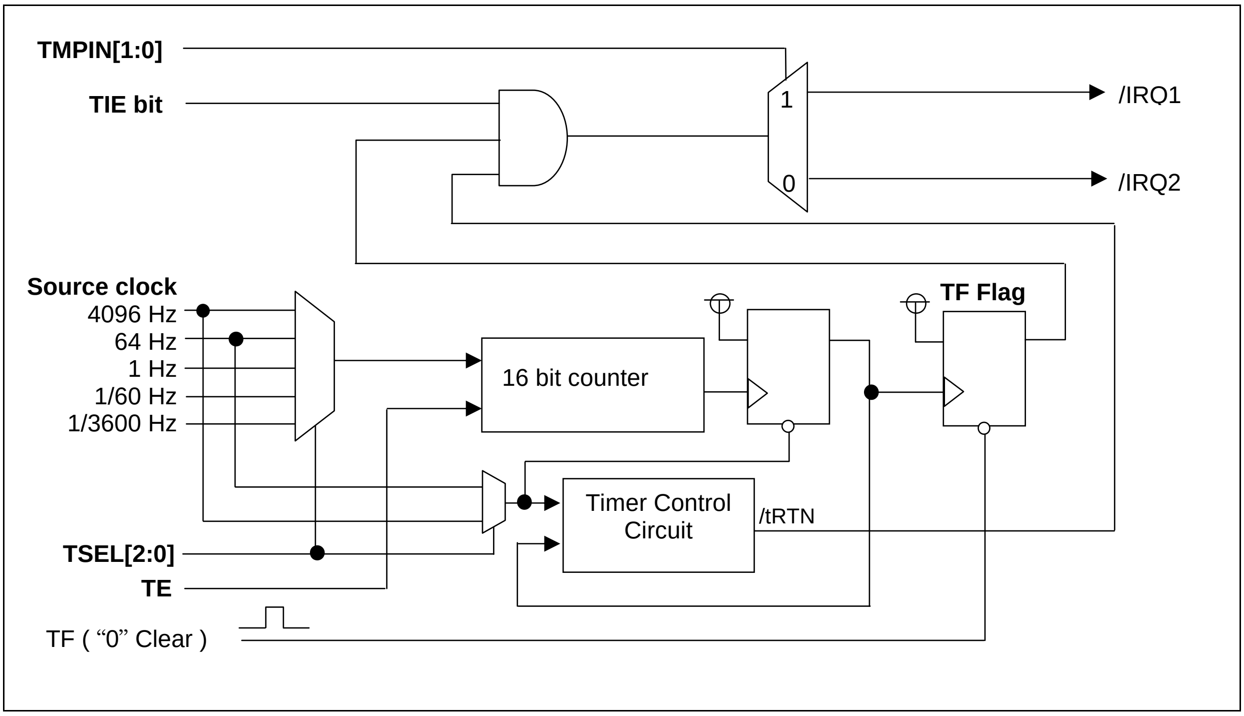


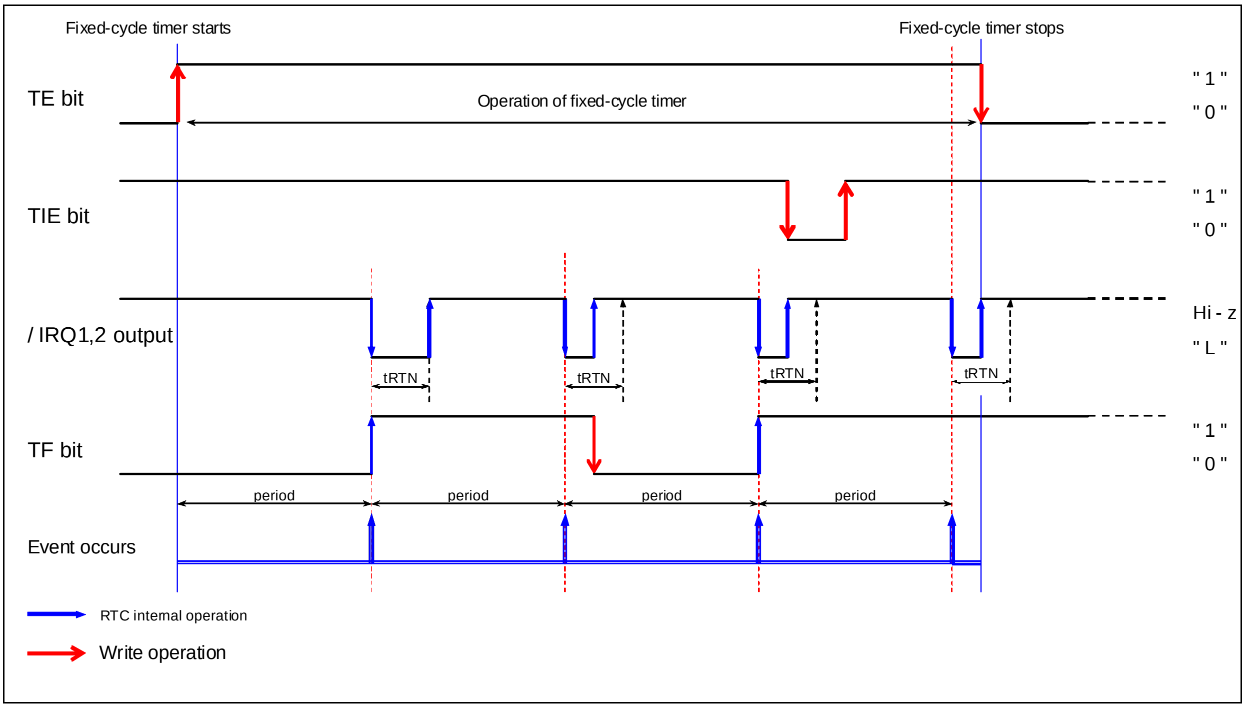
13.2.4. Fixed-cycle timer interrupt interval (example)

The combination of the source clock settings and fixed-cycle timer countdown setting sets interrupt interval, as shown in the following examples.

Timer Counter setting 1 ~ 65535	Source clock				
	4096 Hz TSEL2 = 0 TSEL1, 0 = 0, 0	64 Hz TSEL2 = 0 TSEL1, 0 = 0, 1	1 Hz TSEL2 = 0 TSEL1, 0 = 1, 0	1 / 60 Hz TSEL2 = 0 TSEL1, 0 = 1, 1	1 / 3600 Hz TSEL2 = 1 TSEL1, 0 = 0, 0
0	–	–	–	–	–
1	244.14 µs	15.625 ms	1 s	1 min	1 h
:	:	:	:	:	:
410	100.10 ms	6.406 s	410 s	410 min	410 h
:	:	:	:	:	:
3840	0.9375 s	60.000 s	3840 s	3840 min	3840 h
:	:	:	:	:	:
4096	1.0000 s	64.000 s	4096 s	4096 min	4096 h
:	:	:	:	:	:
65535	15.9998 s	1023.984 s	65535 s	65535 min	65535 h

13.2.5. Diagram of fixed-cycle timer interrupt function





- ∗ After the interrupt event that occurs when the count value changes from 0001h to 0000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)
- ∗ The count down that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

13.3. Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ1 pin goes to low level to indicate that an event has occurred. AF bit and IRQ output change after 1.46ms from alarm agreement at the maximum.
∗ /IRQ1="L" output when occurs alarm interruption event is not cancelled automatically unless giving intentional cancellation and /IRQ1="L" is maintained.

13.3.1. Related registers for Alarm interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
18	MIN Alarm	**AE**	40	20	10	8	4	2	1
19	HOUR Alarm	**AE**	•	20	10	8	4	2	1
1A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1D	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	UF	TF	**AF**	○	VLF	○
1F	Control Register	***TEST***	STOP	UIE	TIE	**AIE**	TSTP	-	-

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.
∗ When the STOP bit value is "1" alarm interrupt events do not occur.
∗ When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
∗ Even if use alarm register as RAM register, inside of RTC is processed as alarm setting, therefore it is able to prevent unintentional alarm occurrence (/IRQ1="L" occurrence) due to unexpected agreement with writing data and timer condition by means of setting to AIE="0".

1) Alarm registers (Reg – 18[h] to 1A[h])

In the WEEK alarm /Day alarm register (Reg - 1A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

∗1) The register that "1" was set to "AE" bit, doesn't compare alarm.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 1A):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only an hour and minute accords with alarm data.

∗2) If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

∗3) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

2) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ1 low output to be canceled (/IRQ1 remains Hi-z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	–
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ1 pin when an Alarm interrupt event has occurred.

AIE	Data	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ1 status remains Hi-z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ1 status changes from low to Hi-z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ1 status changes from Hi-z to low).

∗The AIE bit is only output control of the /IRQ1 terminal. It is necessary to clear an AF flag to cancel alarm.

13.3.2. Examples of alarm settings

1) Example of alarm settings when "Week" has been specified (and WADA bit = "0")

Week is specified WADA bit = "0"	Week Alarm								HOUR Alarm	MIN Alarm
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S		
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07 h	AE bit = 1
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	AE bit = 1	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

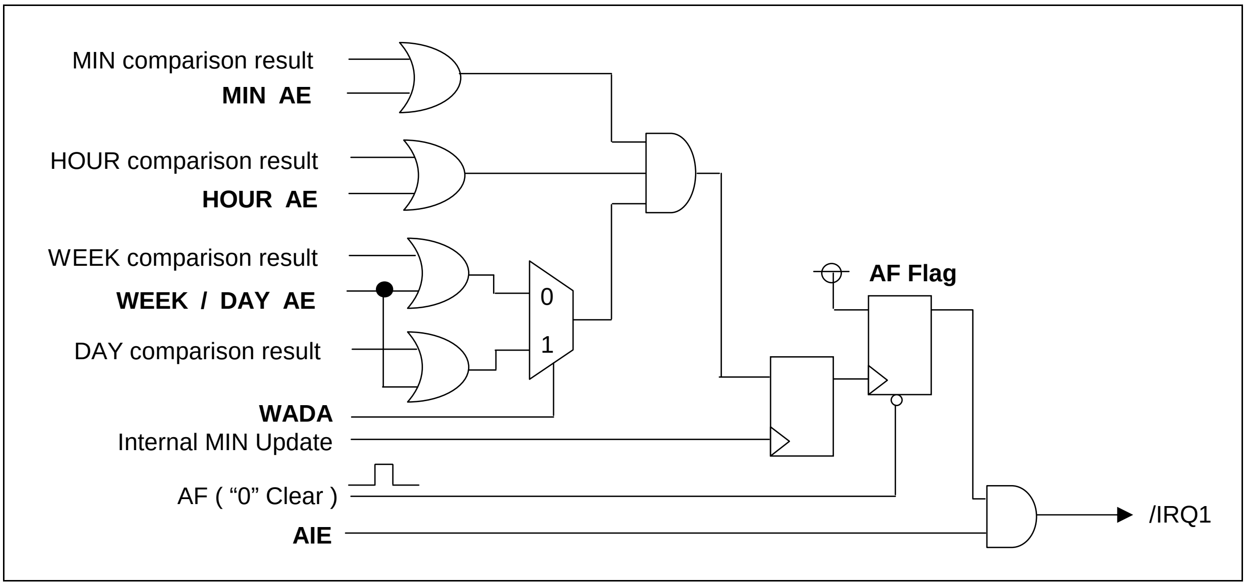
X: Don't care

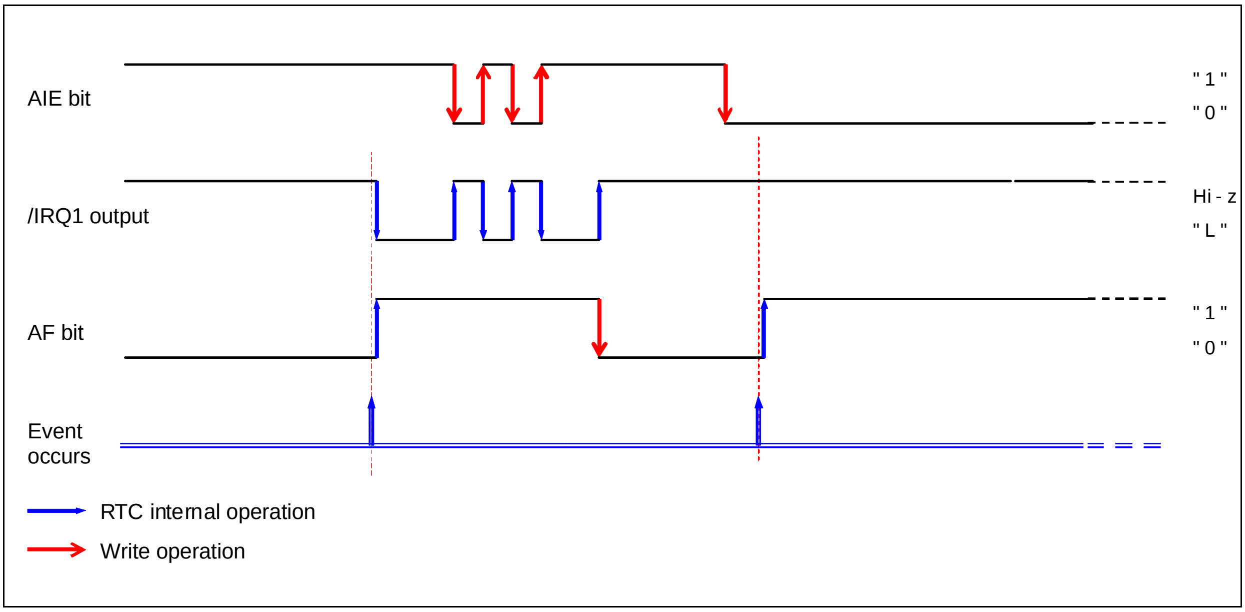
2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Day Alarm								HOUR Alarm	MIN Alarm
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01		
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	07 h	AE bit = 1
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	AE bit = 1	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

13.3.3. Diagram of alarm interrupt function





13.4. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock. This /IRQ1 status is automatically cleared

13.4.1. Related registers for time update interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	TSEL2	TSEL1	TSEL0
1E	Flag Register	○	○	**UF**	TF	AF	○	VLF	○
1F	Control Register	***TEST***	STOP	**UIE**	TIE	AIE	TSTP	-	-

∗ Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" time update interrupt events do not occur.

∗ Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /IRQ1 pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

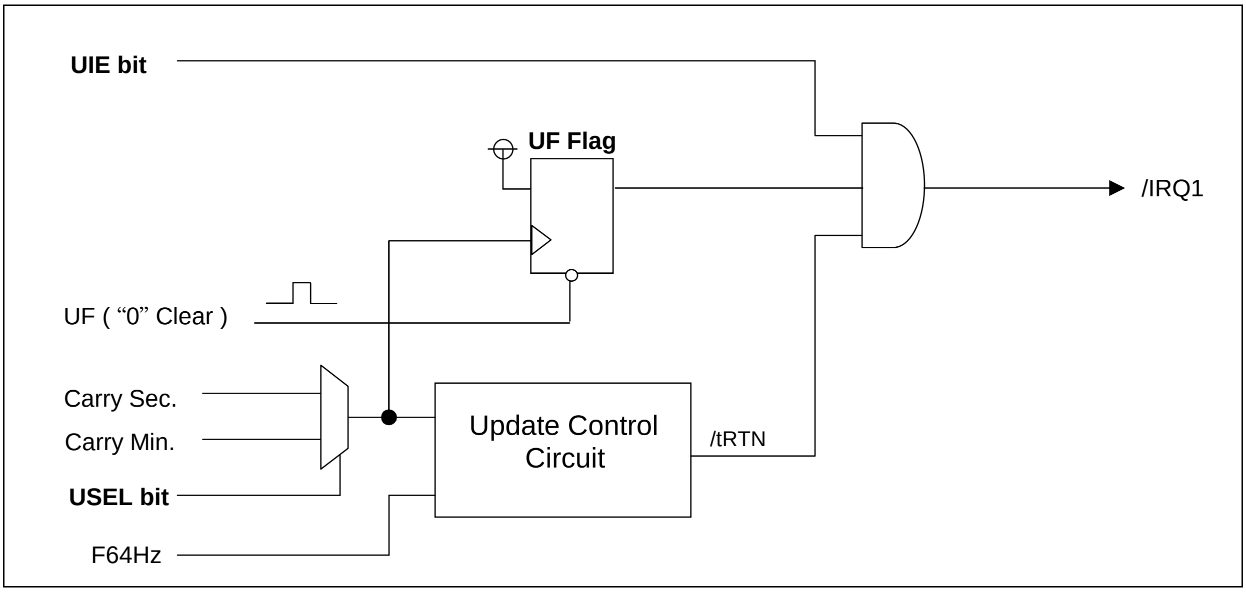
UF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ1 low output to be canceled (/IRQ1 remains Hi-z) when an time update interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	–
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

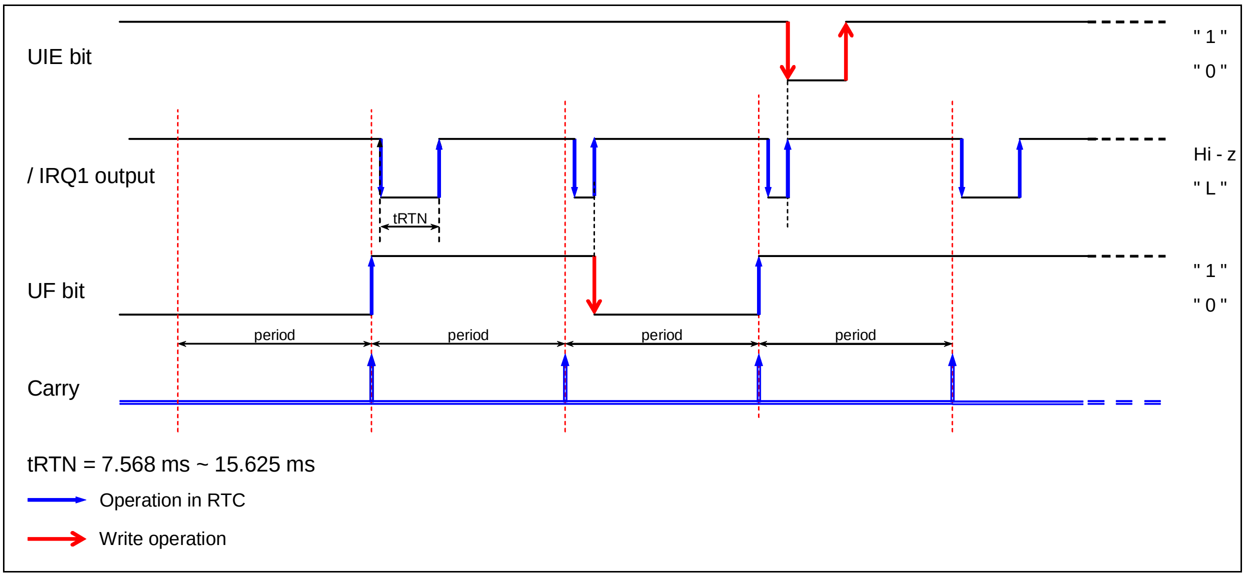
3) UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

UIE	Data	Description
Write / Read	0	1) Does not generate an interrupt signal. (/IRQ1 remains Hi-z) 2) Cancels interrupt signal triggered by time update interrupt event (/IRQ1 changes from low to Hi-z).
	1	When an Update interrupt event occurs, an interrupt signal is generated.

13.4.2. Time update interrupt function diagram





13.5. Frequency stop detection function

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.This function can not detect voltage down of short time.
During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.

VLF	Data	Description
Write	0	The VLF is cleared to 0, and waiting for next low voltage detection.
	1	It is impossible to write in 1 to VLF.
Read	0	RTC register data are valid.
	1	RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

13.6. FOUT function [clock output function]

The clock signal can be output via the /IRQ1, /IRQ2 pin.
When stopped the /IRQ2 pin output, the pin becomes the Hi-z.

13.6.1. FOUT control register.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	TSEL2	TSEL1	TSEL0

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
32	IRQ Control	○	-	-	-	○	TMPIN	**FOPIN1**	**FOPIN0**

By a combination of FSEL1,FSEL0, an FOUT outputs 32768Hz and 1024Hz and 1Hz and can stop the output.

13.6.2. FOUT function table.

FOUT output pin layout and select the frequency.

FOPIN1	**FOPIN0**	Output pin	FSEL1	FSEL0	output
0	0	/IRQ2 (CMOS)	0	0	OFF
			0	1	1 Hz Output
			1	0	1024 Hz Output
			1	1	Don't set it
0	1	/IRQ1 (Open-Drain)	0	0	OFF
			0	1	1 Hz Output
			1	0	1024 Hz Output
			1	1	32768 Hz Output32768 Hz Output

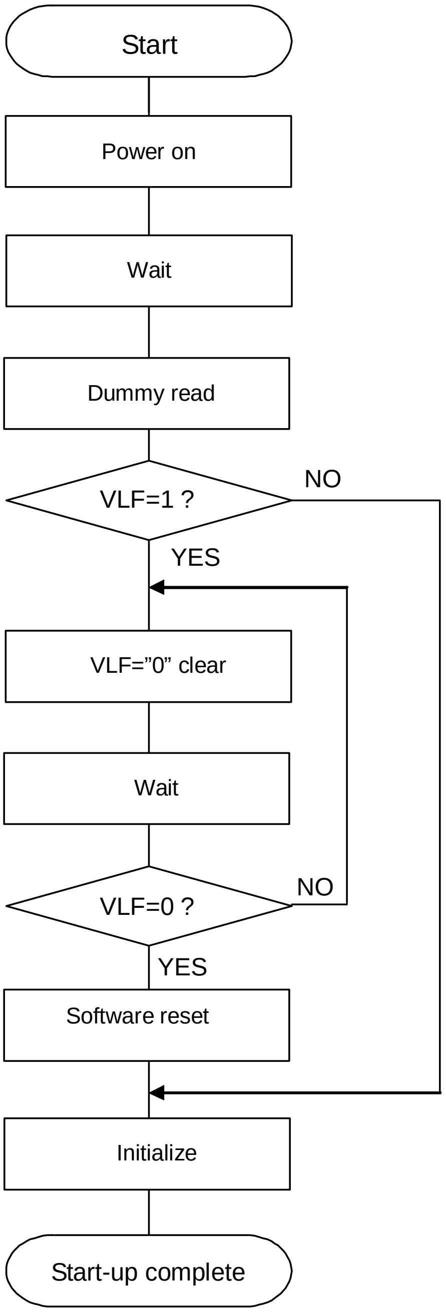
∗ At the time of the initial power-on, “0” is set to FSEL1, FSEL0.

Note: The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz output is possible.
But 1Hz and 1024Hz output is disabled.

13.7. Flow-chart

The following flow-chart is one instance.
Mention for easy understanding takes precedence over others; therefore there are some inefficient cases for the actual processing. If you wish to take more efficient process, perform some processes at the same time or try to confirm and adjust some part where is no hindered from transposing of operation procedure. (Unnecessary processing may be included in mentioned items according to conditions to use.
To get movement according to your expectation, please surely adjust according to conditions to use (use environment).

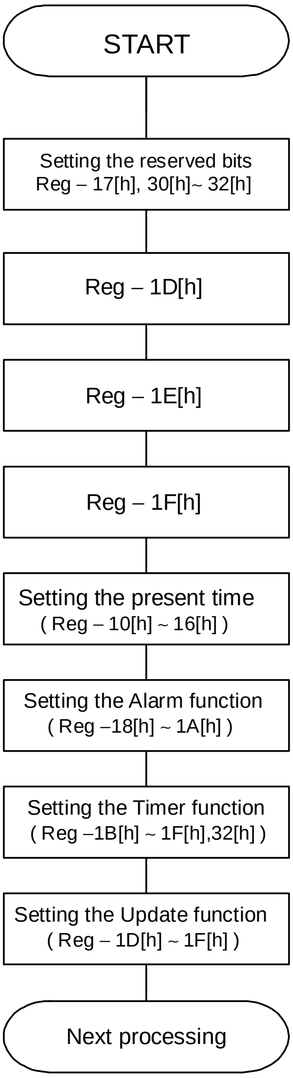
1) Processing example of the power on.



- Wait time of 40ms is necessary at least
- When power-on reset cannot satisfy a power supply condition valid, execute a dummy read.
- Whether it is a return from the state of the backup is confirmed.
- When an internal oscillation starts, 0 writing of VLF is approved.
- Please set waiting time depending on load of a system optionally
- When power-on reset cannot satisfy a power supply condition valid, execute a software reset.
  After software reset, VLF bit is set "1" again.

2) An example of the initialization

Ex.1 Initialize



- Reserved bits have to write in specified fixed value in the case of initialization by all means.

- Set TE bit to “0”.
- Set FSEL1, 0 bit optionally.

- Clear VLF bit to “0”.

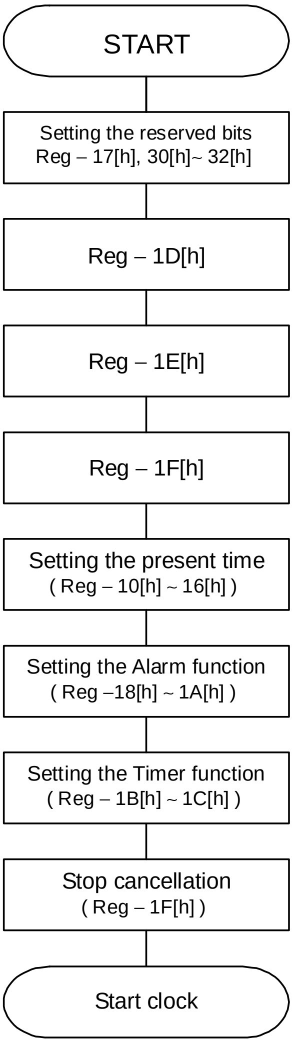
- Surely set TEST bit to " 0 ".
- Set AIE, TIE, UIE bit to “0 " to prevent unprepared interruption output.

- Set the present time.
  ∗ Setting the present time concerned, please refer to item of [Clock and calendar writing] .

- Set the Alarm interrupt function.
  When the alarm interrupt function is not being used, the Alarm registers (Reg - 18h to 1Ah) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
- Set the fixed-cycle Timer function.
  When the fixed-cycle timer function is not being used, the fixed-cycle timer register (Reg – 1B to 1C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.
- Set the Update interrupt function.

∗ When initialization is finished, be sure to set STOP bit to “0”.

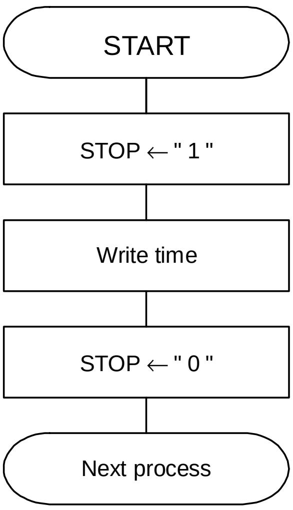
Ex.2 This example is use only for clock functions.



- Reserved bits have to write in specified fixed value in the case of initialization by all means.
- Write 04[h]
- Write 00[h]
- Write 40[h]
  Set STOP bit to “1” to prevent timer update in time setting.
- Set the present time.
- The alarm function stops by initialization of Reg 1F[h].
  Reg - 18h to 1Ah can be used as a RAM register.
- The Timer function stops by initialization of Reg - 1E[h] and Reg – 1F[h].
  Reg – 1Bh to 1Ch can be used as a RAM register.
- Write 00[h]
  Cancel STOP bit to “0” and start (restart) clock.

∗ When initialization is finished, be sure to set STOP bit to “0”.

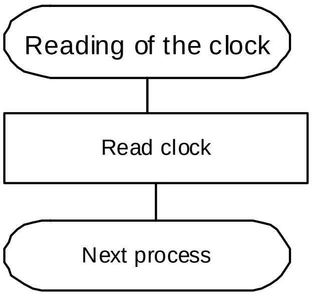
3) The setting of a clock and calendar



- Set STOP bit to “1” to prevent timer update in time setting.
- Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset).
  In case of initialization, please initialize all data.
- Cancel STOP bit to “0” and start (restart) timer movement.
  Timer is started when set STOP bit to “0”.

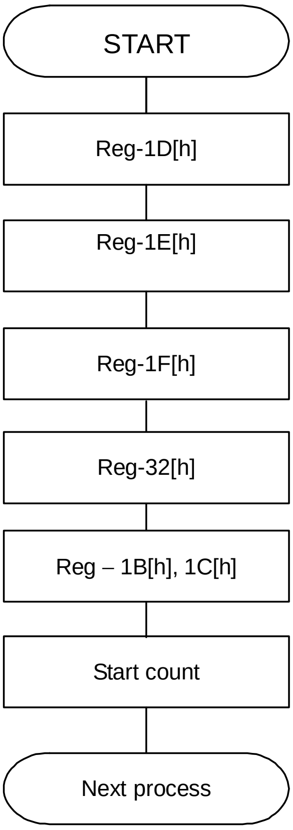
∗ It is able to set time even if not combined use of STOP bit.
Please note that [clock is started at the time of writing [second]] in case STOP bit is not used.

4) The reading of a clock and calendar



- Please complete access within 0.95 seconds
  The STOP bit holds "0".
  (It causes the clock delay to set STOP bit to "1")
- At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.
- The access to a clock calendar recommends to have access to continuation by a auto increment function.

5) The setting example of the fixed-cycle timer interrupt function



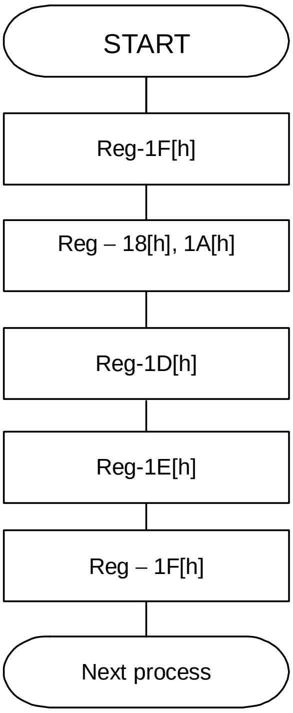
- Clear TE bit to "0" to stop timer-interrupt function.
- The countdown period is fixed by the combination of the TSEL2, TSEL1, TSEL0 bit.
- Clear TF bit to "0" to cancel last timer interrupt output (/IRQ output).
- Select and set /IRQ output
  (if output "L" level interrupt output or not) when event occurs.
  If output "L" level interrupt output, set TIE bit to "1".
- Select output pin. (/IRQ1 or /IRQ2)
- Set initial value of down counter.
- Set TE bit to "1" to start timer interrupt function.

When start timers interrupt function, please surely set/reset (*implement 2) initial value of down counter in advance.

∗1 Countdown is suspended with TSTP, " 0 " → " 1 " and countdown is performed again with TSTP, " 1 " → " 0 "

∗2 When you want to restart from a pre-set value, please set a TE bit to "1" again after setting a TE bit to "0".

6) The setting example of the Alarm interrupt function



- Clear AIE bit to “0” to stop Alarm-interrupt function.
- Set alarm data.
- Select week or day in WADA bit
- Clear AF bit
- Select and set /IRQ1 output in AIE bit.

13.8. Reading/Writing Data via the I²C Bus Interface

13.8.1. Overview of I²C-BUS

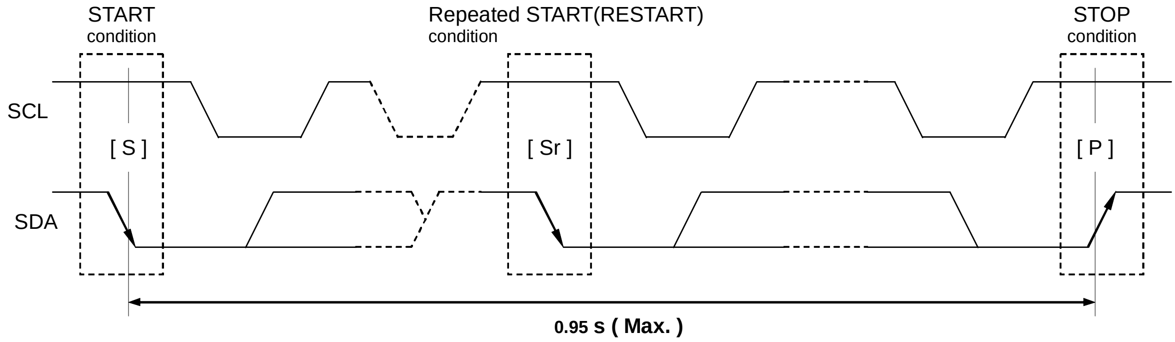
The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

13.8.2. Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(However, the transfer time must be no longer than 0.95 seconds.)

13.8.3. Starting and stopping I²C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition
- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition
- This condition regulates how communications on the I²C -BUS are terminated.
The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)

- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

13.8.4. Slave address

The I²C-BUS devices do not have any chip select or chip enable pins. All I²C-BUS devices are memorized with a fixed unique number in it. The chip selection on the I²C-BUS is executed, when the interface starts, the master device send the required slave address to all devices on the I²C-BUS. The receiving device only reacts for interfacing, when the required slave address is agreed with its own slave address.

During in actual data transmission, the transmitted data contains the slave address and the data with R/W (read/write) bit.

Slave address							R/W bit
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1	1	0	0	1	0	R/W

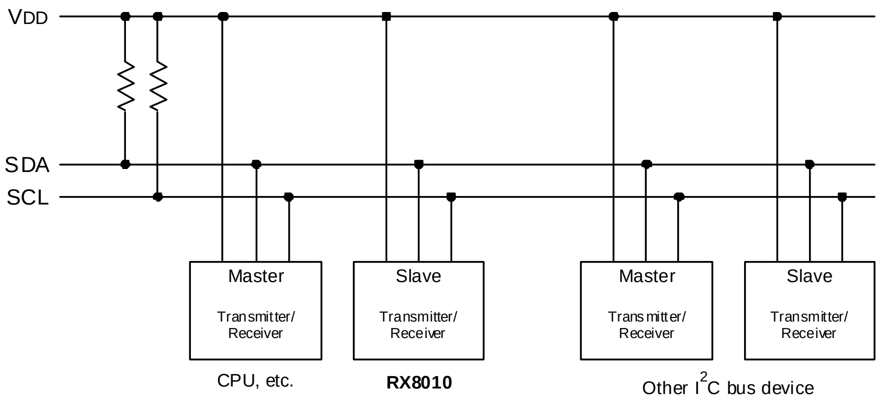
Slave addr : 0x32

0 when write mode
1 when read mode

13.8.5. System configuration

All ports connected to the I^2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VIO line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Any device that controls the data transmission and data reception is defined as a "Master".
and any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

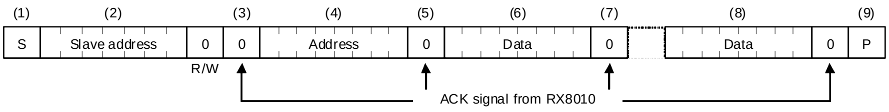
13.8.6. I²C bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RX8010 is the slave.

1) Address specification write sequence

Since the RX8010 includes an address auto increment function, once the initial address has been specified, the RX8010 increments (by one byte) the receive address each time data is transferred.

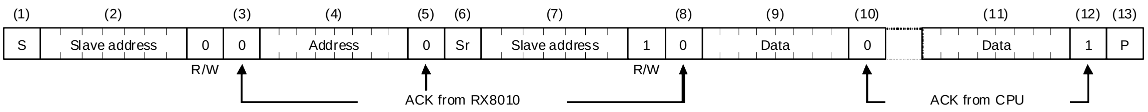
(1) CPU transfers start condition [S].
(2) CPU transmits the RX8010's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8010.
(4) CPU transmits write address to RX8010.
(5) Check for ACK signal from RX8010.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RX8010.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



2) Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

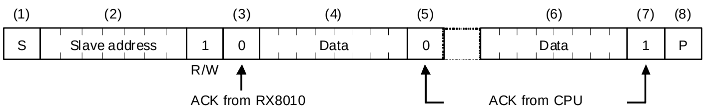
(1) CPU transfers start condition [S].
(2) CPU transmits the RX8010's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8010.
(4) CPU transfers address for reading from RX8010.
(5) Check for ACK signal from RX8010.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RX8010's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RX8010 (from this point on, the CPU is the receiver and the RX8010 is the transmitter).
(9) Data from address specified at (4) above is output by the RX8010.
(10) CPU transfers ACK signal to RX8010.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].



3) Read sequence when address is not specified

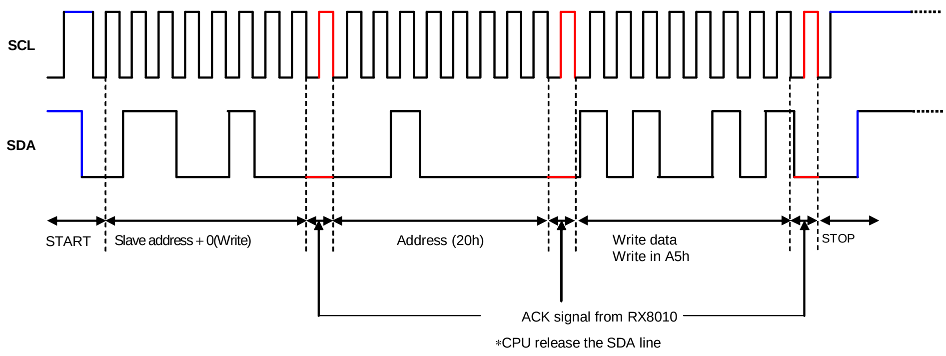
Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8010's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RX8010 (from this point on, the CPU is the receiver and the RX8010 is the transmitter).
(4) Data is output from the RX8010 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RX8010.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RX8010.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].

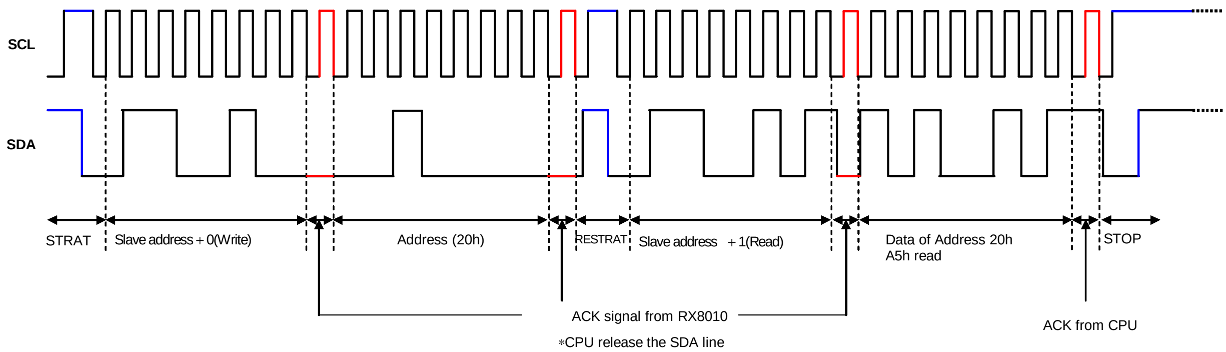


13.8.7. The example of the communication wave pattern

1) Address specification read sequence
When write in A5h for address 20h:



2) Address specification read sequence
When read A5h from address 20h:



Application Manual

AMERICA

Epson Electronics America, Inc.

Headquarter
214 Devcon Drive, San Jose, CA 95112, U.S.A.
Phone: (1)800-228-3964
FAX :(1)408-922-0238
http://www.eea.epson.com

Chicago Office
1827 Walden Office Square. Suite 520 Schaumburg, IL 60173, U.S.A.
Phone: (1)847-925-8350
Fax: (1)847 925-8965

El Segundo Office
1960 E. Grand Ave., 2nd Floor, El Segundo, CA 90245, U.S.A.
Phone: (1)800-249-7730 (Toll free) : (1)310-955-5300 (Main)
Fax: (1)310-955-5400

EUROPE

Epson Europe Electronics GmbH

Headquarter
Riesstrasse 15, 80992 Munich, Germany
Phone: (49)-(0)89-14005-0 Fax: (49)-(0)89-14005-110
http://www.epson-electronics.de

ASIA

Epson (China) Co., Ltd.

Headquarter
7F, Jinbao Building No.89 Jinbao Street Dongcheng District, Beijing, China, 100005
Phone: (86) 10-8522-1199 Fax: (86) 10-8522-1120
http://www.epson.com.cn/ed/

Shanghai Branch
High-Tech Building,900 Yishan Road Shanghai 200233,China
Phone: (86) 21-5423-5577 Fax: (86) 21-5423-4677

Shenzhen Branch
12/F, Dawning Mansion,#12 Keji South Road, Hi-Tech Park,Shenzhen, China
Phone: (86) 755-2699-3828 Fax: (86) 755-2699-3838

Epson Hong Kong Ltd.

Unit 715-723 7/F Trade Square, 681 Cheung Sha Wan Road, Kowloon, Hong Kong
Phone: (86) 755-2699-3828 (Shenzhen Branch)
Fax: (86) 755-2699-3838 (Shenzhen Branch)
http://www.epson.com.hk

Epson Taiwan Technology & Trading Ltd.

14F, No.7, Song Ren Road, Taipei 110
Phone: (886) 2-8786-6688 Fax: (886)2-8786-6660
http://www.epson.com.tw/ElectronicComponent

Epson Singapore Pte. Ltd.

No 1 HarbourFront Place, #03-02 HarbourFront Tower One, Singapore 098633.
Phone: (65)- 6586-5500 Fax: (65) 6271-3182
http://www.epson.com.sg/epson_singapore/electronic_devices/electronic_devices.page

Seiko Epson Corporation Korea Office

19F (63Bldg.,Yoido-dong) 50, 63-ro, Yeongdeungpo-gu, Seoul, 150-763, Korea
Phone: (82) 2-784-6027 Fax: (82) 2-767-3677
http://www.epson-device.co.kr

SEIKO EPSON CORPORATION

Distributor

Electronic devices information on WWW server

http://www5.epsondevice.com/en/quartz/index.html